

EDN

Part 1—Designer's guide to
floating-point processing

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development stations

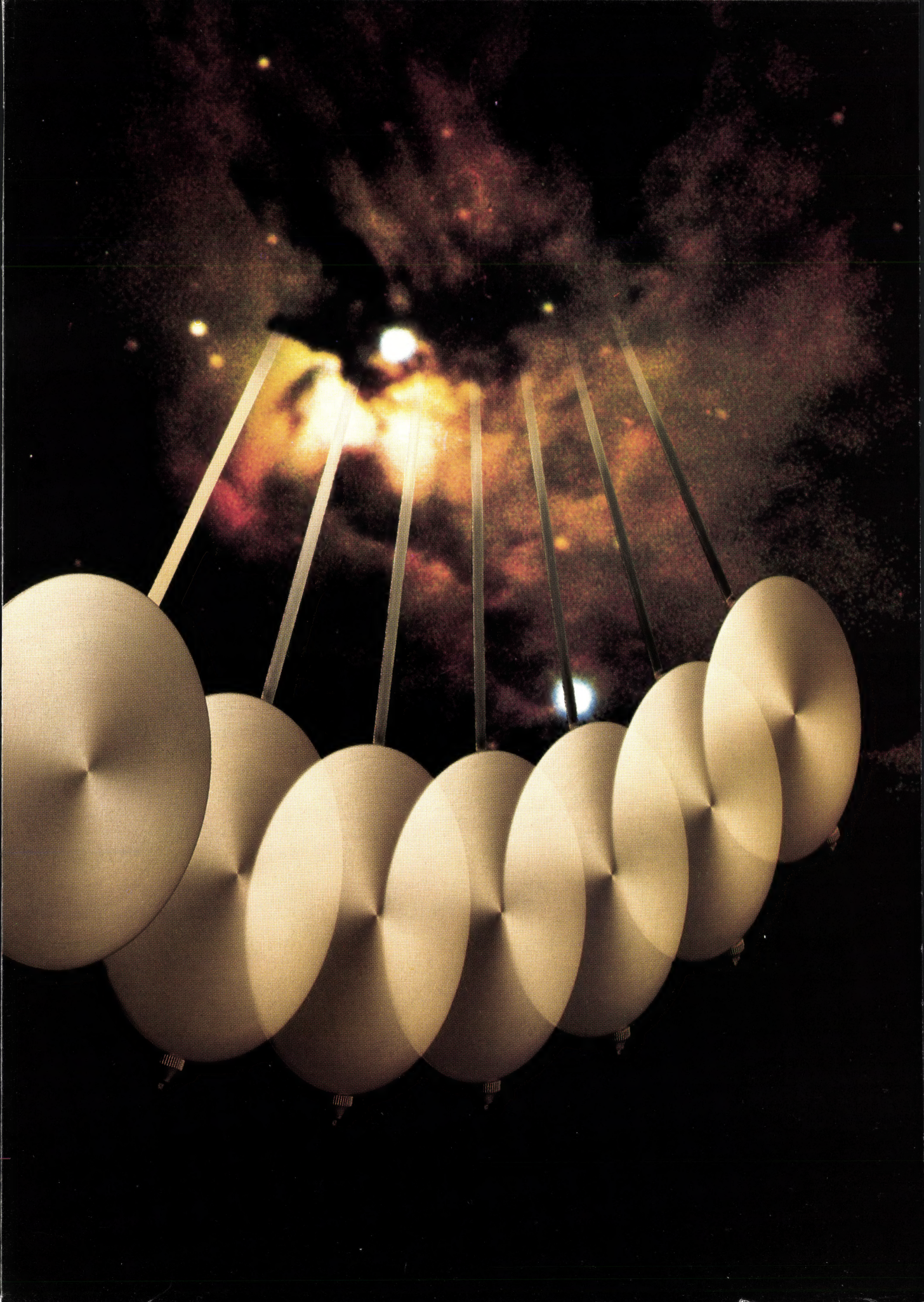
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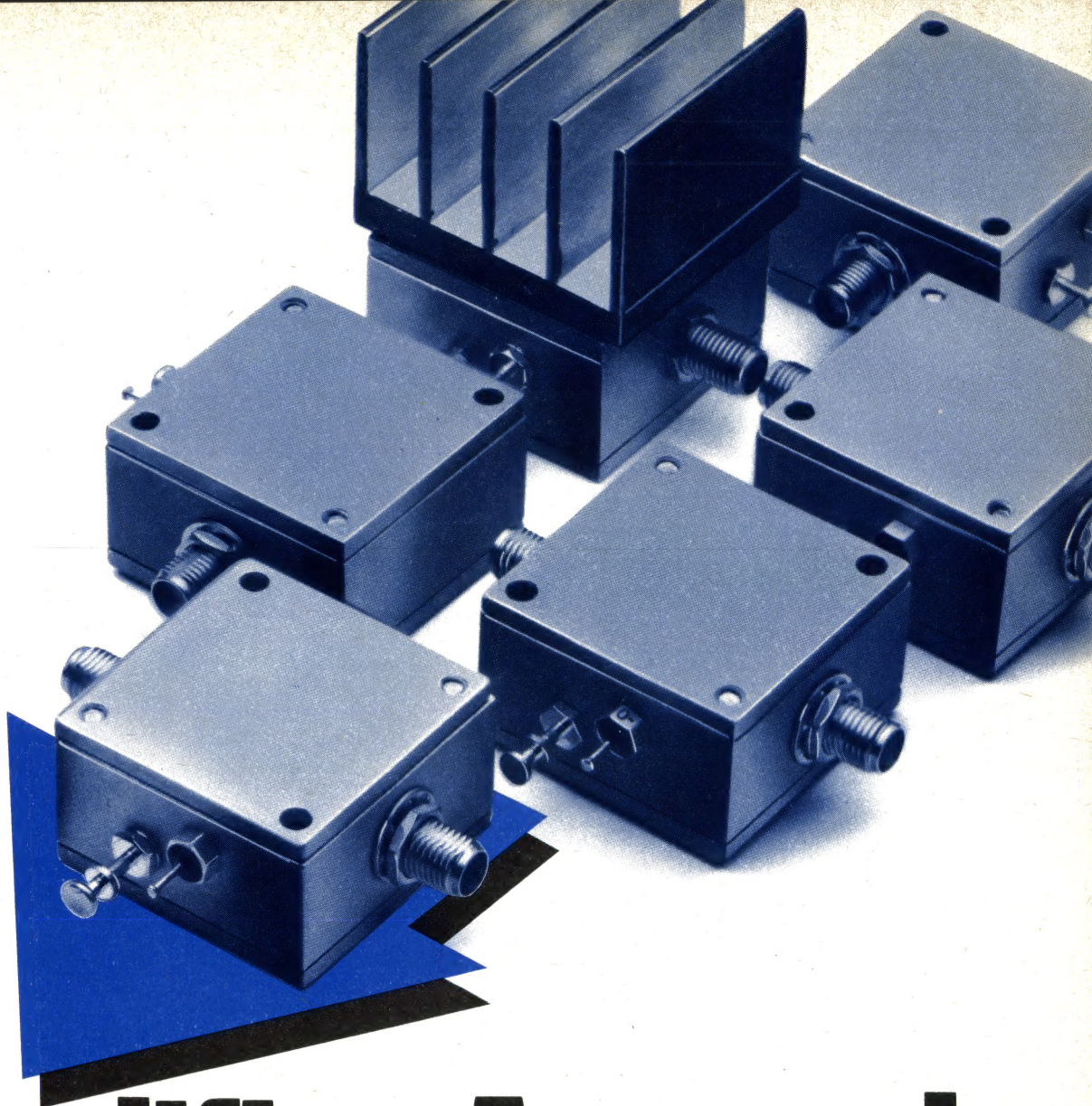


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Gain Flatness (dB) Max.	±1.0	±1.5	±1.5	±1.0
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NF (dB) typ.	5.3	12.0	7.0	5.0
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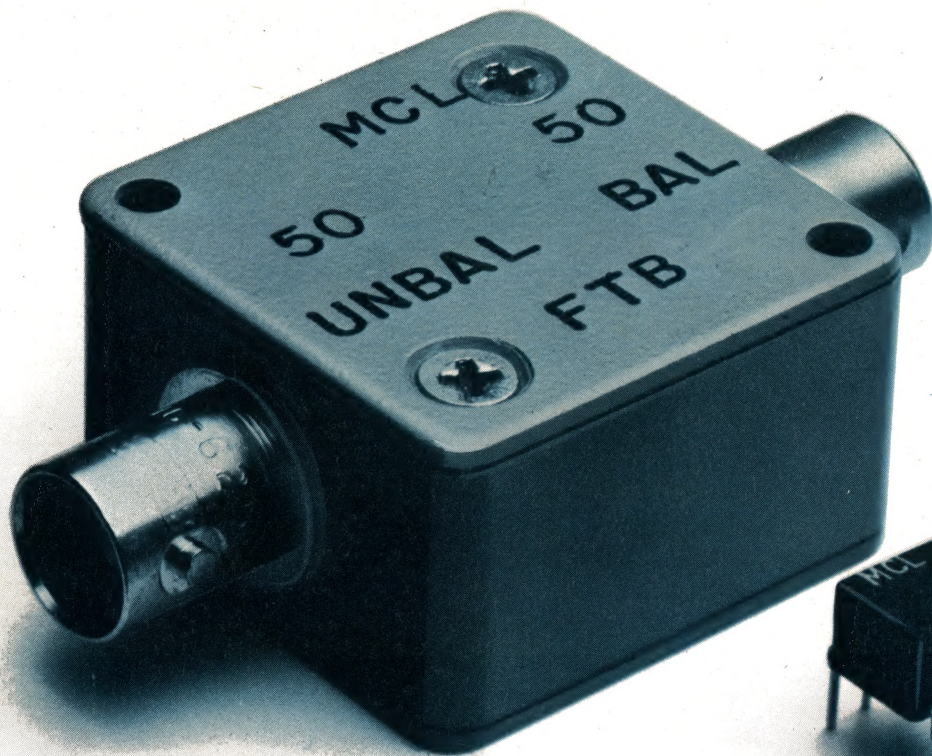
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CIRCLE NO 4



On the cover: You can simplify your designs by choosing μ Cs with on-chip options such as A/D converters, serial peripheral and control interfaces, DTMF generators, display drivers, and pulse-width modulators. See pg 90. (Photo courtesy Toshiba)

DESIGN FEATURES

Special Report: Enhanced 1-chip μ Cs 90

Choosing among today's enhanced 1-chip μ Cs, which offer an ever-expanding array of options, can be more difficult than choosing a large computer. The chips range from 4-bit devices with limited ROM to sophisticated 16-bit μ Cs with many features.

Designer's Guide to: Floating-point processing—Part 1 115

Floating-point arithmetic gives you better dynamic range and precision than integer arithmetic, but it needs careful implementation. Part 1 of this 3-part series discusses possible sources of error you may encounter when using floating-point hardware, and it reviews the current standards.

Test your analog-design IQ—Part 2 127

Midterm break is over; it's time to test your skill with 25 entirely new linear-design challenges, some of which have deliberately planted bugs. Designed with more recent ICs than those in Part 1, these circuits reflect modern-day speed and stability problems.

High-speed EDAC memory uses PROMs instead of EDAC ICs 141

If your memory-cycle requirements are tighter than the performance specs for commercially available error-detection and -correction chips, then a faster, PROM-based scheme may suit your needs. There's only one restriction: You'll have to build your memory arrays out of 8-bit-wide segments.

Answers to EDN's analog-IQ quiz—Part 2 155


With the realization that the answers might be debatable, get ready to score Part 2 of your analog-design quiz.

EDN Technical-Article Database Index 169

EDN's semiannual database index lists major articles published from May through October 1985 in EDN, Electronic Design, Electronics, Electronic Products, and Computer Design.

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The memory interface provides access to a linear 4 Gbyte address space at a data transfer rate of up to 25 Mbytes/sec.

Transputers are designed for ease of engineering. All transputer family devices operate from a single 5 MHz clock input, which is used to derive high speed internal clocks for all on chip systems.

When transputers are directly connected via links, additional components are not necessary. Independent or common clocking can be used, regardless of timing skew.

The configurable memory controller also requires no external components. It provides all

the necessary timing and refresh signals for memory systems, comprising any mix of ROM, SRAM, DRAM and memory mapped peripherals.

Transputers are designed for ease of programming. INMOS offers development systems which provide integrated editing, compiling and source level debugging for both single and multiple transputer applications, using C, Pascal, Fortran and occam.

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Systems of any size can be built from inter-connected transputers, using the links. The same program can be configured to run on one, tens or thousands of transputers allowing a simple trade off between performance and cost.

The transputer family already includes 32 bit and 16 bit transputers, peripheral controllers, evaluation boards and development tools. Start assessing its capability for yourself now with an IMS T414 evaluation board.

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IMS T212	16 Bit, 2 Kbyte RAM, 4 Transputer links
IMS C001	Transputer Link Adaptor, Separate 8-Bit input and output
IMS C002	Transputer Link Adaptor, Multiplexed 8-Bit input/output

DEVELOPMENT TOOLS

IMS D100	INMOS Transputer Development System
IMS D600	Transputer Development Software, VAX-VMS
IMS D700	Transputer Development Software, IBM-PC

EVALUATION BOARDS

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IMS B004	IBM-PC add on card, IMS T414, 1 Mbyte RAM

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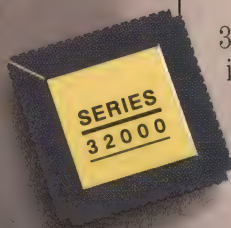
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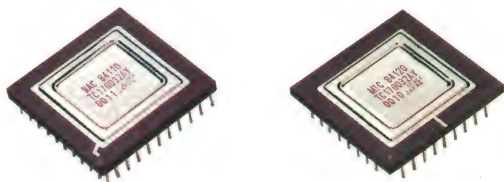
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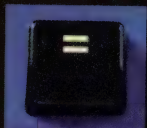
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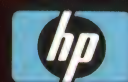
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NEWS BREAKS

EDITED BY JOAN MORROW

6809 INTERPRETER / DEBUGGER RUNS ON IBM PC

Able to run on any IBM PC or PC-compatible computer, the \$299 AVSIM09 program from Avocet Systems Inc (Rockport, ME) interprets and executes 6809 μ P programs under control of a screen-oriented symbolic debugger. The screen displays register and flag information as well as program- and data-memory contents. Editing keys let you manipulate the on-screen information, and function keys let you set breakpoints, switch to single-step operation, and start programs. The simulator's trace memory provides a record of recent operations, so you can back up through a program to isolate bugs. The debugger portion of the program simulates operations of 6821 programmable interface adapter (PIA), 6840 programmable timer module (PTM), and 6850 asynchronous communications interface adapter (ACIA) I/O and control chips. By simulating the I/O devices, the AVSIM09 program tests your software on the IBM PC without forcing you to load the software into your 6809-based target system from the IBM PC.—Jon Titus

INDUSTRY-STANDARD AND HIGH-SPEED ADCs GO MONOLITHIC

Available for the first time in a single-chip version, the industry-standard AD574A 12-bit A/D converter from Analog Devices Inc (Norwood, MA) comes in a 28-pin plastic DIP and costs \$27.90 (100). According to the manufacturer, the IC is the industry's first complete ADC to include a microprocessor interface, clock, and reference on one chip. The converter has 3-state output buffers that allow a direct interface with 8-, 12-, or 16-bit buses. Another monolithic A/D converter, Analog Devices' AD7572, is the industry's fastest 1-chip, 12-bit ADC. The device offers 5- μ sec max conversion time and dissipates 165 mW max—a fraction of the power dissipated by comparable-speed hybrid converters. The ADC achieves its speed by using npn transistors in the comparator's input stage. The linear-compatible CMOS LC²MOS process allows the fabrication of a buried zener reference, making the IC the only CMOS A/D converter that has an on-chip reference. Available in 20-pin plastic or ceramic single DIPs, the converters cost \$35 to \$197.50 (100).—Bill Travis

512k-BIT EPROM PROGRAMMER CHECKS, VERIFIES DEVICES

The EPROM-1, the second device in a series of low-cost programmers from International Microsystems (Auburn, CA, (916) 885-7262), programs EPROM/EEPROM devices with as much as 512k bits. The \$495 programmer includes error-checking routines to ensure correctly socketed and programmed parts. Its 64k \times 8-bit data RAM can be expanded to 128k \times 8 bits. The \$495 ECL-1 programmer, which was introduced last summer, includes a copy of National Semiconductor's PLAN PLD development software and programs all of National's and MMI's ECL PLDs.—Chris Everett

SPEED-ENHANCEMENT MODULE ACCELERATES PC PERFORMANCE BY 60%

Accelerating the performance of any IBM PC or PC-compatible computer by as much as 60%, Fast88 from Microspeed Inc (Fremont, CA, (408) 748-8630) doesn't affect the computer's software compatibility. Any software that ran before you installed Fast88 will still run, but more quickly. The module replaces the standard 8088 CPU with a higher-speed 8088-2 or optional NEC V20 and then lets you switch the system clock between the standard 4.77 MHz and 6.2, 6.7, or 7.4 MHz. The choice of clock rate depends on the limits of the system's RAM and EPROM. The \$129.95 Fast88 includes a 2 \times 3.5-in. pc board, CPU chip, external control module with speed-select switch and reset button, cables, documentation, and installation instructions.—Ed Teja

NEWS BREAKS

COMPANY TO DUPLICATE BIT-SLICE μ Ps IN CMOS

With plans to produce CMOS equivalents of the entire line of 2900 Series bit-slice μ Ps, Integrated Device Technology (IDT) (Santa Clara, CA, (408) 727-6116) has launched its first 4-bit μ P in the Microslice family of microprogrammable devices. Functionally compatible and pin-compatible with the 2901C, the IDT39C01C is fabricated with the company's 1.2- μ m CEMOS-II process under the direction of John Mick, who originally developed the 2900 Series bit-slice line for Advanced Micro Devices (Sunnyvale, CA). Operating at one-fifth the power of its bipolar counterpart and in full compliance with MIL-STD-883 Method 5004, military-grade samples of the IDT39C01C are available in either 40-pin DIPs or 44-pin LCC packaging for \$45 (100). The commercial cerdip version costs \$12 (100).

IDT also offers the 12-bit IDT39C10B and the 16-bit IDT49C410 microprogram sequencers as CMOS replacements for 2910A devices. These ICs consume less than one-third the power (440 mW) of the bipolar 2901A with the same output drive capability and feature a microprogram address register, direct external input, internal register/counter, and a 33-deep LIFO stack. The cerdip commercial versions of the IDT39C10B and IDT49C410 cost \$18.60 and \$24.80 (100), respectively; military versions are priced at \$58.80 and \$78.40 (100), respectively.—Denny Cormier

ARCHITECTURE ELIMINATES LOWPASS FILTER'S ERROR CONTRIBUTION

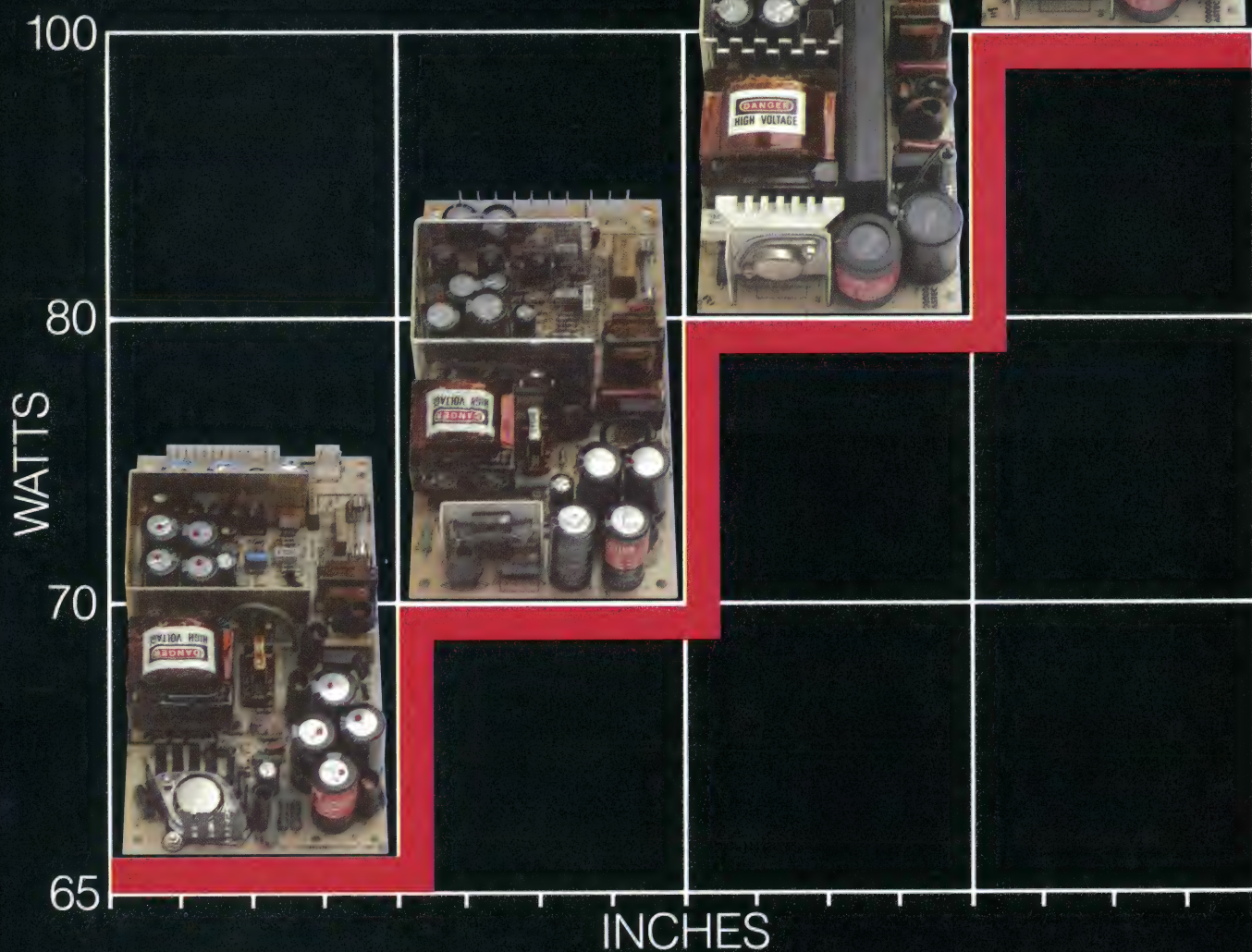
A switched-capacitor lowpass filter from Linear Technology Corp (Milpitas, CA) makes no contribution to a system's dc offset voltage or low-frequency noise. The \$3.55 (100) LTC1062's architecture places the device outside the system's dc signal path. A fifth-order, all-pole, maximally flat filter, the IC uses an internal clock frequency that you can set by selecting an external capacitor; you could also use an external clock whose frequency is as high as 4 MHz. Clock-to-cutoff frequency ratio is typically 100:1. The filter provides attenuation of 30 and 60 dB at two and four times the cutoff frequency, respectively. You can connect two LTC1062s in cascade to obtain a tenth-order lowpass-filter characteristic. Operating from 5 to 18V (total span) single or dual supplies, the CMOS device is housed in an 8-pin DIP and draws 7-mA supply current.—Bill Travis

HIERARCHICAL RAM COMBINES STATIC-, DYNAMIC-RAM DESIGN

By combining ECL static-RAM and CMOS dynamic-RAM designs onto one chip, Visic Inc (San Jose, CA, (408) 945-9991) has created the V16H4/41 (16k \times 4-bit) high-speed HRAM (hierarchical RAM). Working from one 5V supply voltage, the /41-35 version boasts a maximum access time of 35 nsec and dissipates only 315 mW of power. A static-column mode permits an access time of 25 nsec for a 256-bit word.

Alternate sources for the part will be Monolithic Memories Inc (65C16H4/41) and VLSI Technology Inc (VT16H4/41). You can receive sample quantities now; the manufacturer expects the price for production quantities will be \$20 (10,000) for the /41-55 version in either a 28-pin, 400-mil DIP (V16H41) or in a space-saving 24-pin, 300-mil DIP (V16H4).—Denny Cormier

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20dB Stop Band start from	70	135	210	290	410	580	750	800	1000	1100	1340

HIGH PASS Model PHP	-50	-100	-150	-200	-300	-400	-500	-600	-700	-800	-900	-1000
Passband, MHz start stop	41 200	90 400	133 600	185 800	290 1200	395 1600	500 1600	600 1600	700 1800	780 2000	910 2100	1000 2200
20dB Stop Band, (MHz) from DC to	26	55	95	116	190	290	365	460	520	570	660	720

OCCASIONALLY, EVERYONE WISHES HE HAD ANOTHER SHOT AT HIS DESIGN.

There are some things man was not meant to tamper with.

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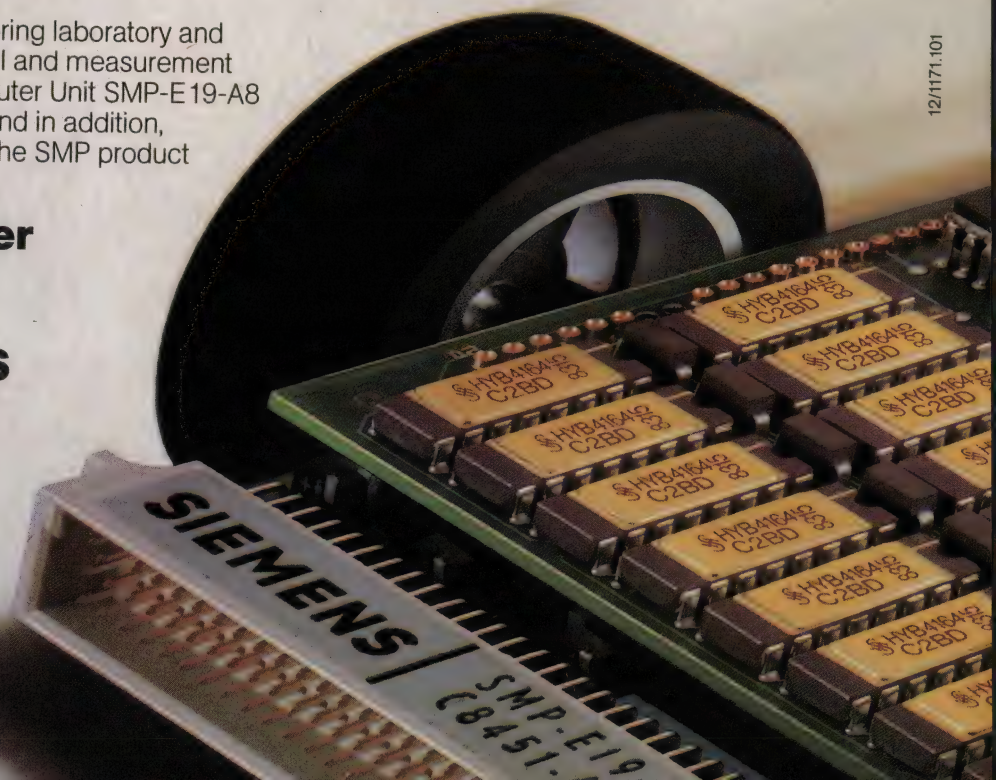
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SIGNALS & NOISE

Support policies make no sense

Dear Editor:

A very belated comment on your editorial "The cost of support: Reasonable or a rip-off?" (EDN, August 23, 1984, pg 65): Amen! Even when companies have the best of intentions and warranties, it's silly to have to send or take a product to them when the only repair needed is the replacement of a \$.25 IC.

Further, present-day technology makes the availability of programming information as important as the availability of hardware information. One manufacturer actually refused to provide me with programming information on the grounds that such information was proprietary! I wasn't asking for hardware- or programming-design information, but only for sufficient information about the hardware to write my own programs to work

with the company's hardware. In another case, I asked the manufacturer of a "preprogrammed" industrial product to provide enough programming information so that I could reprogram the product for my application. The manufacturer responded to the effect that the information is in the hardware manuals; good luck, and don't bother to ask for any help.

A hardware-repair situation that has me puzzled involves a printer I own. I found, upon inquiry, that the printer had to be shipped to the manufacturer's repair facility, which is in the Boston area. The shipping costs and time required made this solution unacceptable. I located a nearby independent repair company, which happened to be an authorized repair agent for the printer manufacturer. For reasons that I fail to understand, the supposedly independent company

would not perform nonwarranty repairs without authorization from the manufacturer. This situation came to naught, but I have the feeling that something akin to (illegal) restraint of trade is involved.

*Sincerely yours,
Everett M Greene
Ridgecrest, CA*

IEEE P981 proposal is not yet a standard

Dear Editor:

Peter Harold's article on the IEEE P981 task force's draft standard ("New IEEE-488 bus specs promise to ease systems integration and enhance performance," EDN, September 19, pg 97) is misleading. Mr Harold begins the article by saying, "If the recommendations of the P981 task force are accepted as a new set of IEEE standards, you can

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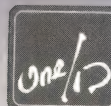


- generation of serial and revision numbers
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SIGNALS & NOISE

look forward to significantly lower costs for IEEE-488 systems integration and applications-program generation." He then goes on to describe the draft proposal as if it were, for all intents and purposes, complete and fixed.

The draft standard is not complete, nor is it accepted even by the full task force, let alone the rest of the IEEE or the industry. Though I am not a formal member of the task force, I have had the opportunity to review most of the draft and to make comments through task-force members. Many people who are involved in the development of IEEE-488-compatible instruments believe that the current P981 draft has significant weaknesses that are yet to be resolved.

Mr Harold's discussion of device trigger timing is one example of a function that's still under debate. He states that the proposed change would "make it easier to synchronize operation of an instrument with the application program running on the system controller." This statement refers to a part of the draft that specifies that Group Execute Trigger (GET) messages be queued through the instrument's input buffer, just as are device-dependent commands. The fact is that the proposed change solves one problem and creates another.

Queuing a GET message allows a user to send the GET message directly following a device-dependent command; the message will not be executed until the device-dependent commands have been processed. However, the queuing scheme also introduces timing uncertainty into the execution of GET messages. If you send GET messages to several instruments simultaneously, you can't be sure when individual instruments will execute the GET instructions unless you first check that the instruments have all finished processing device-dependent commands. This status checking is exactly what the proposed improve-

ment to GET messages was intended to eliminate.

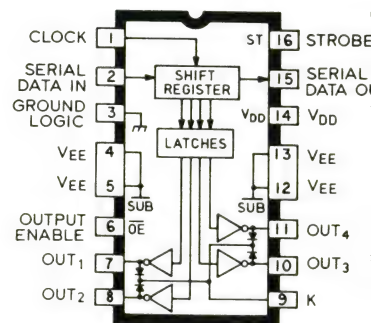
Not only does the proposed GET execution scheme pose problems, but implementing the scheme is not as trivial a matter as the article suggests. Mr Harold asserts that "it shouldn't be difficult for instrument designers to place GET instructions into the input queue." The fact is that such special input cases place a significant burden on the GPIB I/O drivers and input parser/scanners in an instrument, and this burden results in lower performance (ie, slower talker/listener data rates).

I have given just one example of the problems with P981. Problems with the device I/O rules and status-byte handling sections also remain unresolved. Although the new standard has the potential to help ease the massive programming burden that's currently on the ATE system programmer, the standard must also be carefully designed to allow for different instrument architectures and future innovation. Otherwise, P981 may meet with a lack of industry enthusiasm, as did the previous IEEE-728 syntax standard.

Although it's important to publish information on new developments like the P981, the press must be careful not to establish de facto standards by encouraging the industry to begin designing to standards that don't exist yet. Otherwise, you'll be setting standards, not reporting on them.

*Sincerely yours,
Mark D Tilden
Design Engineer
Tektronix Inc
Beaverton, OR*

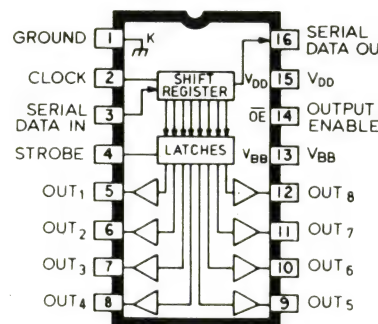
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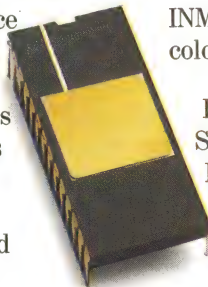
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NEWS BREAKS: INTERNATIONAL

EDITED BY JOAN MORROW

256k-BIT CMOS ROM IS COMPATIBLE WITH TI AND INTEL CHIPS

Ricoh Co has added to its line of 256k-bit CMOS masked ROMs with the high-speed RP23C256H and RP23C257H, which are pin compatible with Intel's 27256 and Texas Instruments' 2564, respectively. These 32k-word×8-bit parts consume 192.5 mW during operation and 110 μ W in standby. The devices operate from one 5V power supply and are available in sample quantities for ¥1000 (\$4.88).

JAPANESE IBM AT-COMPATIBLE COMPUTER TO BE AVAILABLE IN US

Sanyo Electric is expected to introduce an IBM AT-compatible microcomputer in the US this month. The MBC-990 Series will feature an 80286 μ P, 512k bytes of RAM, and a 1.2M-byte floppy-disk drive. The company will offer a 40M-byte hard-disk drive as an option. The computer, which will furnish a 6- or 8-MHz clock speed, will cost less than \$3000.

1-GHz PRESCALER FEATURES LOW POWER CONSUMPTION

Matsushita Electric Industrial Co has developed a GaAs prescaler that uses 3.2 mA of current at a 1-GHz operating frequency. The 1.0×1.2-mm chip integrates 422 field-effect transistors and uses a 5V power supply. It takes 1-GHz signals and reduces them to 1/128th, 1/130th, 1/256th, and 1/258th of the original level. The company said it succeeded in lowering the power-dissipation level by using a heat-treatment process for ion-injection layers and by employing a technique to smooth the boundary walls when fabricating field-effect transistors. Samples of the device, which is designed for use in portable communications equipment, will be available in the spring for approximately ¥3000 (\$14.63).

INTELLIGENT GRAPHICS TERMINAL PRICED AT ¥980,000 (\$4780)

The TS3 intelligent graphics terminal from Ricoh Co is a bit-mapped-type device with a 15-in. CRT and 1024×768-dot resolution. Built around a 68000 processor, the terminal, which costs ¥980,000 (\$4780), has a 2M-byte max memory capacity and incorporates an RS-232C communication interface. It's designed to be used with a variety of computers, including AT&T's 3B2 Series minicomputers.

8-BIT HOME COMPUTER COSTS 40% LESS THAN PREDECESSOR

Nippon Electric Co has introduced a low-cost 8800 Series 8-bit home computer. The PC-8801mkIIFR, which costs ¥99,800 (\$487) and does not include a floppy-disk drive, is 40% lower in price than the older SR model, but it incorporates similar basic functions. The company also announced a higher-end unit, the 8801mkIIMR, which provides two 1M-byte floppy-disk drives and 192k bytes of memory. It also has a 40-character×20-line kanji display, features Japanese word-processing capability, and costs \$1160.

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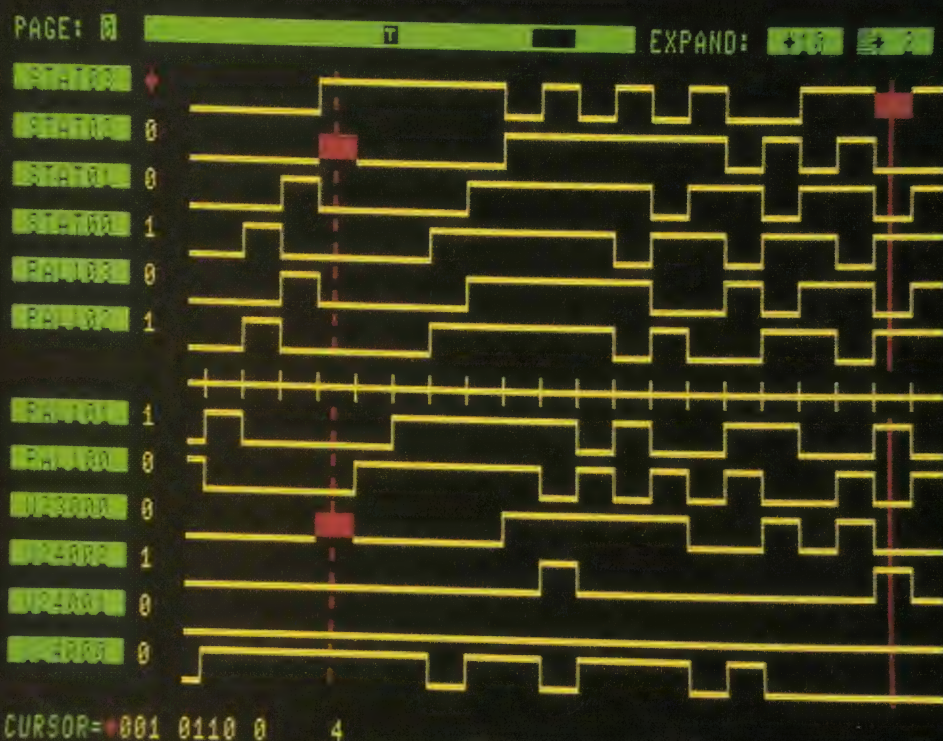
and advantages include high input impedance, good noise immunity, wide logic supply range (5 to 12V), and high data input rates (3 to 5MHz).

Sprague Electric Company, a Penn Central unit, Worldwide Hdqtrs., Lexington, MA. Integrated Circuit Division, Worcester, MA. For applications assistance, call Mark Heisig or Tom Truax at 617/853-5000 or write for Brochure WR-203 to Technical Literature Service, Sprague Electric Company, 41 Hampden Road, Mansfield, MA 02048-1807.



Tektronix

1241 LOGIC ANALYZER



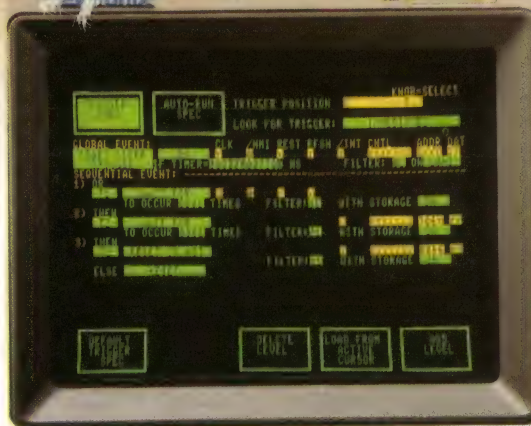
Meet the new 1241—one more reason why Tek's versatile 1200 Series offers you the best of the leading logic analyzers:

1 The 1241's color interface quickly guides your eye to the most relevant information. Analysis is faster. Easier on the eyes. You are more accurate, more productive. For extra readability, a vertical expansion feature doubles the height of the timing diagrams.

2 Like all members of the 1200 Series, the 1241 clearly



shows what your hardware and software are doing at the same time. For integrating partitioned designs, only the 1200 Series' Dual Timebase feature accurately depicts real-time interactions between independently-clocked modules. This lets you monitor relationships between two processors, or between hardware and software. Combine Dual Timebase with performance analysis on the 1241 to analyze the entire system and software performance. Monitor,



for example, the range of time spent by one processor waiting for a service request response from a second processor. The 1241's histogram display and 10ns resolution make these measurements clear and precise.

3 For both hardware and software analysis, Tek offers unsurpassed triggering. Software problems are pinpointed by 14 levels of conditional triggering combined with data and program flow qualification. Triggering on the timing characteristics, as well as the state of the hardware activity, is made possible by counters, timers, and duration filters.

4 Ease of use extends beyond the color screen. Four distinct levels of operation add features as your design challenges require. A unique touch-screen menu display lets you select over 50 high-level commands right off the screen. The big front panel knob provides flicker-free scrolling.

5 Modular, expandable and versatile, Tek's 1200 Series keeps costs low and compromises few. Support

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CIRCLE NO 26 for literature

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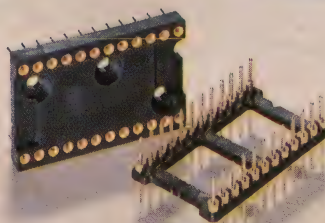


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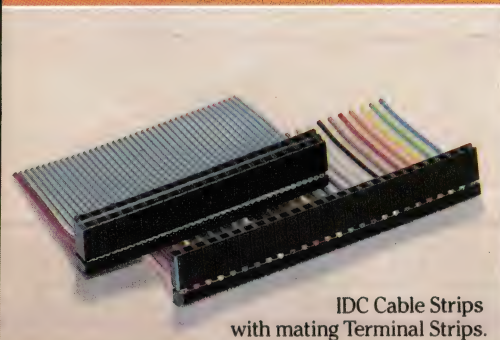


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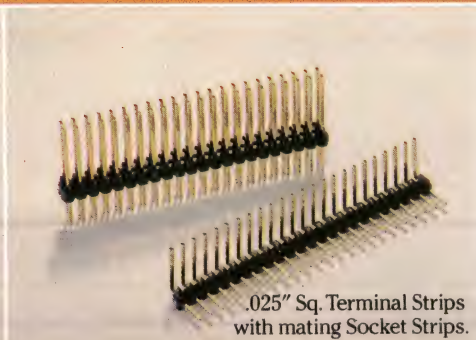
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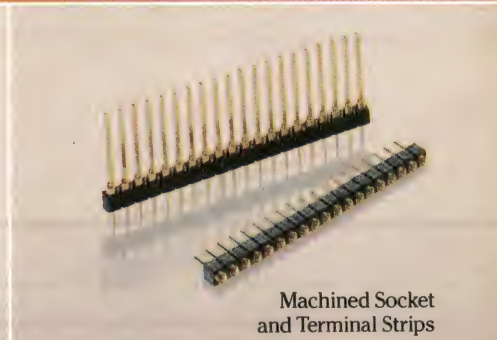
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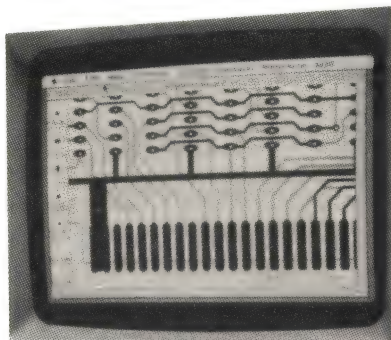
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CIRCLE NO 30

CALENDAR

IBM & AT&T: Local Network Strategic Issues, Washington, DC. Architecture Technology Corp, Box 24344, Minneapolis, MN 55424. (612) 935-2035. January 13 to 14.

SMART II (Surface Mount and Re-flow Technology) (seminar), Los Angeles, CA. Mark Donovan, Electronic Industries Association, 2001 Eye St NW, Washington, DC 20006. (202) 457-4980. January 13 to 16.

Battery Conference on Applications and Advances, California State University, Long Beach, CA. Rita Johnson or Jane Doherty, (213) 498-5102. January 14 to 16.

Buscon/86 (The Bus and Board Conference and Exposition), San Jose, CA. Buscon, 17100 Norwalk Blvd, Suite 116, Cerritos, CA 90701. (213) 402-1618. January 15 to 16.

IBM & AT&T: Local Network Strategic Issues, Phoenix, AZ. Architecture Technology Corp, Box 24344, Minneapolis, MN 55424. (612) 935-2035. January 16 to 17.

Second National Third Party Maintenance Conference, San Diego, CA. Carol Every, Frost & Sullivan, 106 Fulton St, New York, NY 10038. (212) 233-1080. January 21 to 22.

Advanced Semiconductor Equipment Exposition (ASEE) & Technical Conference, San Jose, CA. Cartledge & Associates, 1101 S Winchester Blvd, #M259, San Jose, CA 95128. (408) 554-6644. January 21 to 23.

IBM & AT&T: Local Network Strategic Issues, San Francisco, CA. Architecture Technology Corp, Box 24344, Minneapolis, MN 55424. (612) 935-2035. January 23 to 24.

Investment Opportunities in Telecommunications, Hamilton, Bermuda. IGI Consulting Inc, 214 Har-



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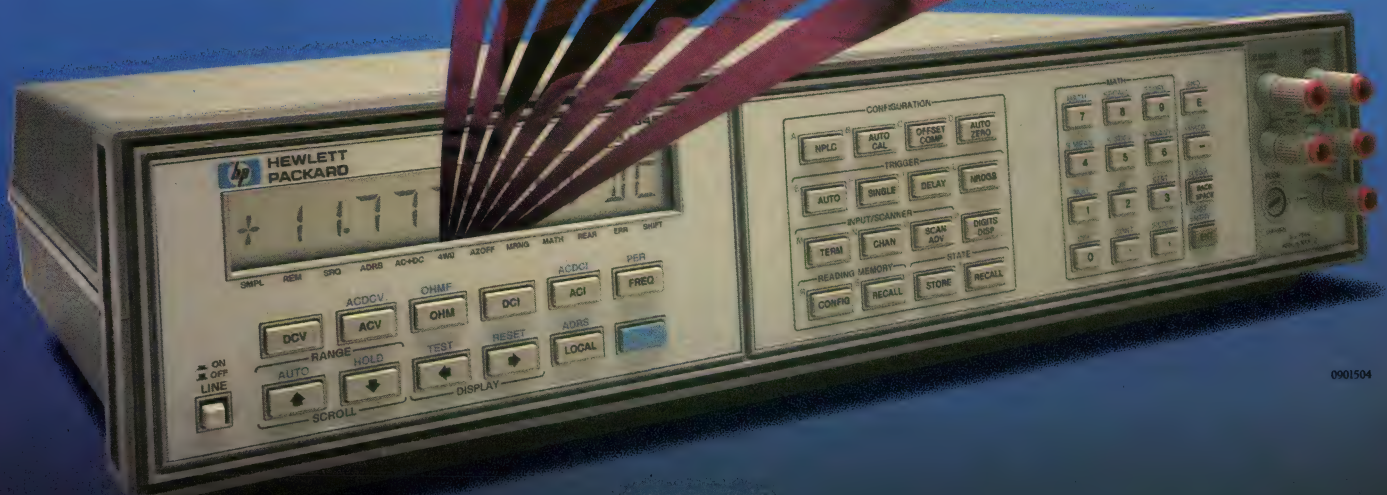
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acV	1 µV	300 V
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acI	10 nA	1.0 A RMS
dcI	100 pA	1.5 A
frequency	10 Hz	1.5 MHz
period	0.1 s	667 ns

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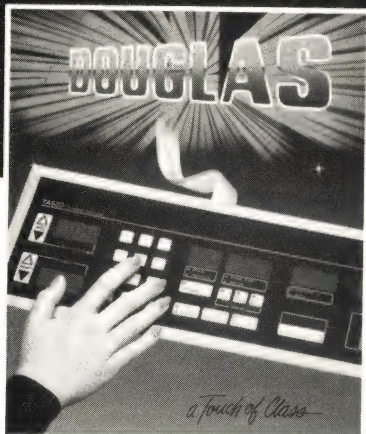
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CIRCLE NO 33

CALENDAR

vard Ave, Suite 200, Boston, MA 02134. (617) 738-8088. January 26 to 29.

Comm/Mart (Communications Marketplace), Washington, DC. CW/Conference Management Group, Box 880, Framingham, MA 01701. (800) 225-4698; in MA, (617) 879-0700. January 27 to 30.

UniForum, Anaheim, CA. /Usr/ Group, 4655 Old Ironsides Dr, Suite 200, Santa Clara, CA 95054. (408) 986-8840. February 4 to 7.

IEEE Annual Meeting, San Jose, CA. IEEE, 10th Fl, 345 E 47th St, New York, NY 10017. (212) 705-7647. February 18 to 19.

Nepcon West '86, Anaheim, CA. Banner and Greif, 110 E 42nd St, New York, NY 10017. (212) 687-7730. February 25 to 27.

Comdex in Japan, Tokyo, Japan. The Interface Group, 300 First Ave, Needham, MA 02194. (617) 449-6600. March 3 to 6.

Compcon Spring, San Francisco, CA. IEEE Computer Society, 1730 Massachusetts Ave NW, Washington, DC 20036. (203) 371-0101. March 3 to 6.

First International Conference on CD ROM, Seattle, WA. Microsoft Corp, Box 97200, Bellevue, WA 98009. (206) 828-8080. March 3 to 6.

Dexpo Europe '86 (DEC-Compatible Exhibition and Conference), London, UK. Expoconsul International, 3 Independence Way, Princeton, NJ 08540. (609) 987-9400. March 4 to 6.

Power UK '86, London, UK. TCM Expositions Ltd, Exchange House, 33 Station Rd, Liphook, Hampshire GU30 7DN, UK. (0428) 724660. March 4 to 6.

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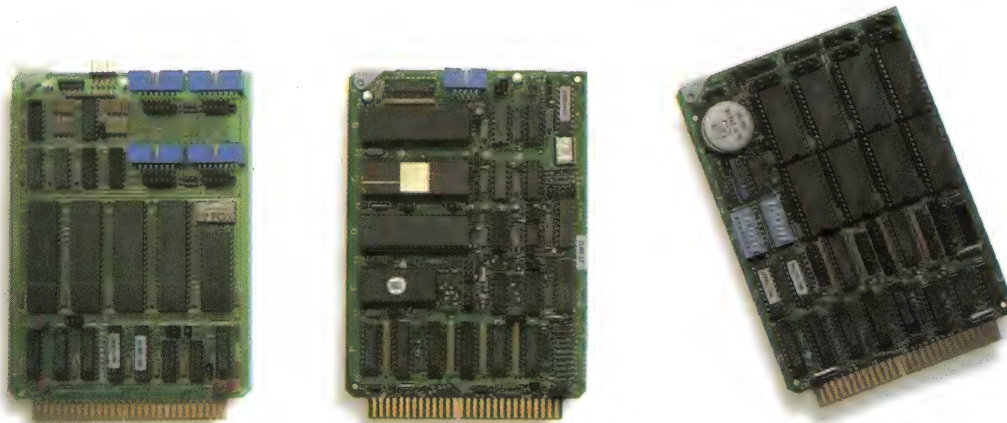


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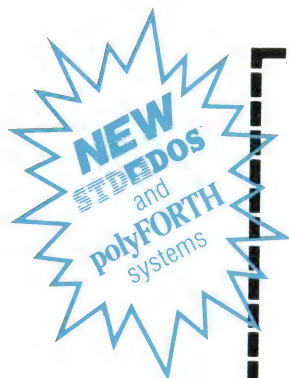
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EDITORIAL

Stick with the business you know; know the business you stick with



Reading Staff Editor Deborah Asbrand's article about innovation in small companies (pg 285) reminded me of the small company I worked for not long after getting my EE degree. My job was to design and develop data-acquisition and -analysis systems for use in sonar and oceanography applications. I felt important and appreciated in this small company, because my projects were a measurable part of the company's business, and their success affected the company's overall success. In fact, both the company and I were doing well.

Then the company was bought by a larger company. This larger company didn't know much about oceanography or sonar, but its officers thought it would be wise to branch out into other businesses. Oceanography and sonar weren't central to any of the larger company's goals, just a hedge against its main business going sour.

Needless to say, my job satisfaction wasn't central to any of that company's goals either. In fact, within a year or two, almost every member of the department I worked in, including myself, became disillusioned and left the company. Soon after that, the company went through some hard times and had some layoffs. The last I heard, it had trimmed down in size and scope and was engaged in only the type of business it had pursued before its diversification.

I relate this personal story only because it conveys a valuable message: Companies (and people, for that matter) should pursue the things they understand and care about, not just anything that shows a potential for making money. If a company must diversify, it should do so with thorough knowledge of, and enthusiasm for, its new area of endeavor.

Unfortunately, the electronics industry is rife with examples of failed ventures in which the participants didn't follow that advice. For every acquisition of an electronics company that has resulted in long-term profitable operation, there seem to be a dozen or more failed or struggling operations in which a helicopter company or an oil company or some other kind of company has just decided, almost casually, to "branch out."

In the last few years, so many companies have "branched out" that conglomeration has run rampant. In one notorious example, two conglomerates even tried simultaneously to buy each other. I can't help but wonder how much better off our economy would be if the efforts that these companies put into planning or preventing takeovers were put to some real use—like developing good products. Companies would be much better off if they would either stick with the things they know or else make it a point to understand very well the things they venture into.

Gary Legg

Gary Legg
Editor

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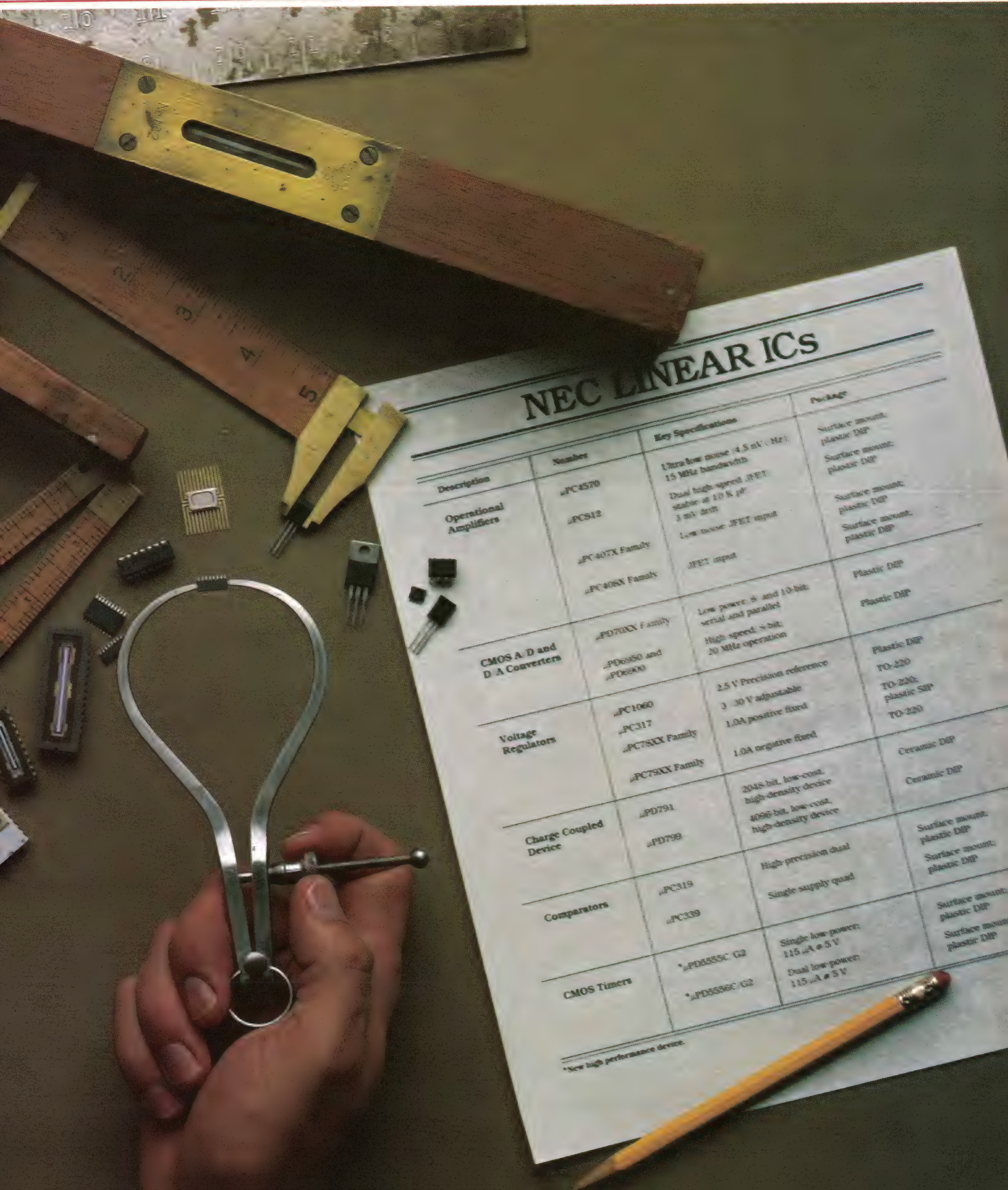
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	μPC512	Dual high-speed JFET stable at 10 K pF 3 mV drift	Surface mount, plastic DIP
	μPC407X Family	Low noise JFET input	Surface mount, plastic DIP
	μPC408X Family	JFET input	Surface mount, plastic DIP
CMOS A/D and D/A Converters	μPD70XX Family	Low power, 8- and 10-bit serial and parallel	Plastic DIP
	μPD6950 and μPD6900	High speed, 8-bit 20 MHz operation	Plastic DIP
	μPC1060 μPC317 μPC78XX Family μPC79XX Family	2.5 V Precision reference 3-30 V adjustable 1.0A positive fixed 1.0A negative fixed	Plastic DIP TO-220 TO-220, plastic SIP TO-220
Voltage Regulators			
Charge Coupled Device	μPD791 μPD798	2048-bit, low-cost, high-density device 4096-bit, low-cost, high-density device	Ceramic DIP Ceramic DIP
Comparators	μPC319 μPC309	High-precision dual Single supply quad	Surface mount, plastic DIP Surface mount, plastic DIP
CMOS Timers	*μPD5555C/G2 *μPD5556C/G2	Single low-power, 115 μA @ 5 V Dual low-power, 115 μA @ 5 V	Surface mount, plastic DIP Surface mount, plastic DIP

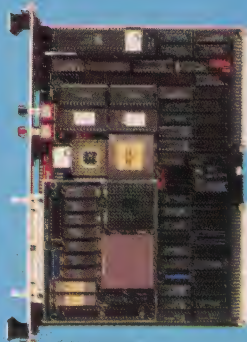
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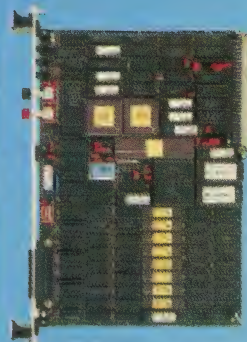
Leadership



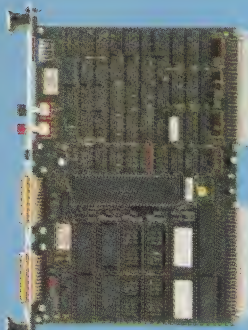
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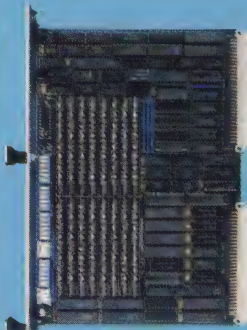
MVME121
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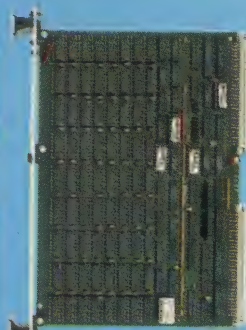
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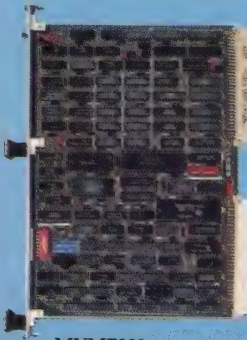
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1MB MVMX32 DRAM



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0.5MB 32-bit DRAM



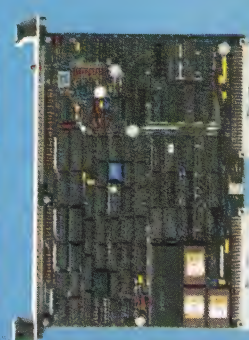
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GPIB 488



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I/O Channel



MVME319
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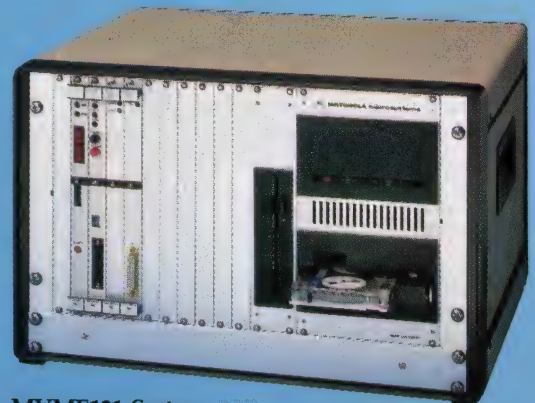


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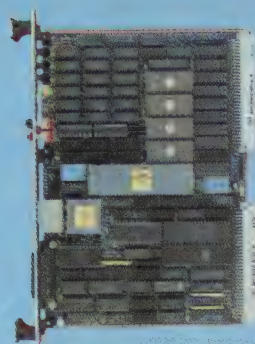


MVME121 System:

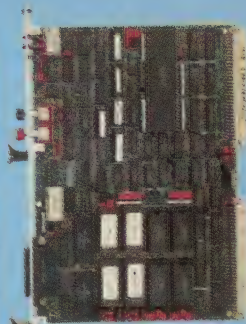
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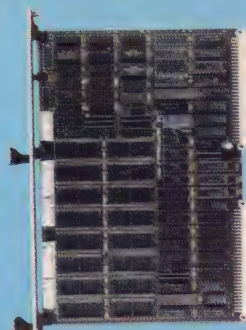
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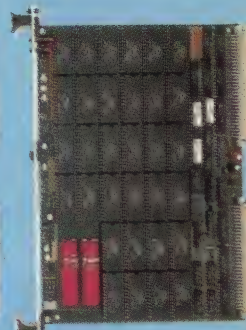
MVME117
MC68010 with MC68881



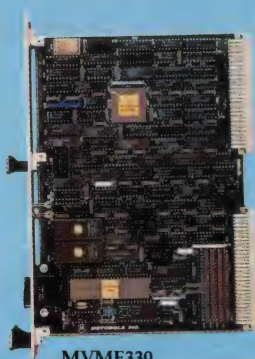
MVME110
MC68000 with I/O Channel



MVME214
MVMX32 ROM



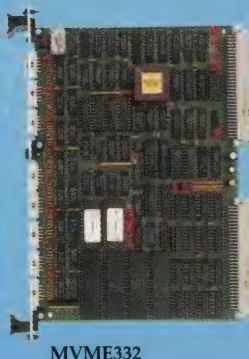
MVME215
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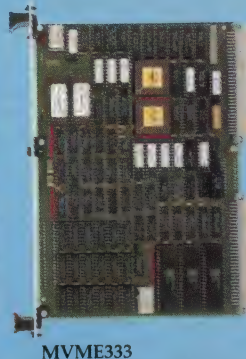
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Ethernet



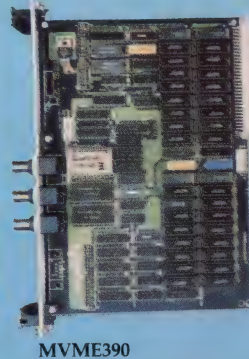
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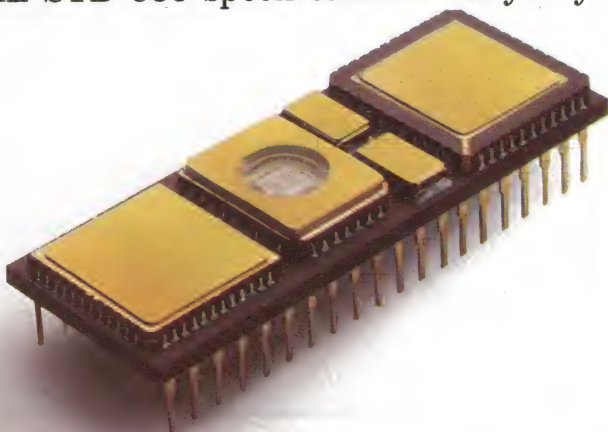
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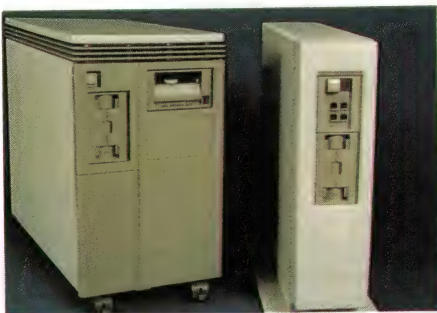
Powerful OEM computer systems double as multiuser software-development stations

Charles H Small, *Associate Editor*

The processing power of high-performance OEM computers based on 16- and 32-bit μ Ps threatens to blur the distinction between a software-development host and the target system. Currently available OEM-computer target systems have enough processing power and high-level software tools to support large software-development projects. They can therefore serve both as development hosts and as target systems for projects involving 16- and 32-bit μ Ps.

Abandoning host-based development and instead doing your software development on examples of your target system—or “going native,” as some refer to the change-over—confers two primary advantages: The OEM target systems can cost less per user than a minicomputer, and, because your software engineers work directly in the target environment, they can develop and test their programs faster and with greater confidence.

Running nearly all software available for DEC's superminicomputers, the MicroVAX II spans a range of configurations, starting with small, single-user systems and overlapping the low end of the superminicomputer field.



Right now, you can obtain from a small number of manufacturers OEM computer systems that, by virtue of their hardware and software configuration, qualify as multiuser development systems. You can expect many more announcements of such systems from other OEM computer houses and IC manufacturers as deliveries and designs of high-performance μ Ps increase.

System configuration is key

The hardware of these systems comprises a 16-bit or (preferably) a 32-bit CPU board, a significant amount of high-speed RAM (1M to 10M bytes), terminal and disk I/O boards, and both floppy- and Winchester-disk drives. The bundled software runs under standard minicomputer operating systems like Unix, VMS, 32-bit Forth, or Regulus, and it includes such sophisticated program-development tools as optimizing compilers, symbolic

debuggers, screen editors that help you with a high-level language's syntax, version-control systems, software-project managers, and real-time kernels.

Costs for currently available development/target systems range from a low of \$6000 to \$20,000 or more. Note that the range of costs neatly spans the gap between a fully loaded personal computer (like an IBM PC/AT) and a minicomputer.

The representative systems listed in Table 1 are available now. Use care when evaluating two of the specs presented: price and number of users. First, the prices quoted may or may not include all the software and hardware you would order. In addition, prices could run higher because these systems are expandable.

Second, the number of users a given system will support depends heavily on the type of software the users are running. Running a compiler, for example, taxes RAM and



Costing little more than a fully loaded personal computer, the \$5995 Microforce-1 from Force Computers Inc is a VME Bus-based OEM computer that can also serve as a 2-user software-development station. It comes with Unix System V (installed) and several compilers. In addition to the operating system, the 68010-based computer includes 1M byte of RAM, a 22M-byte Winchester-disk drive, a floppy-disk drive, and four serial I/O channels.

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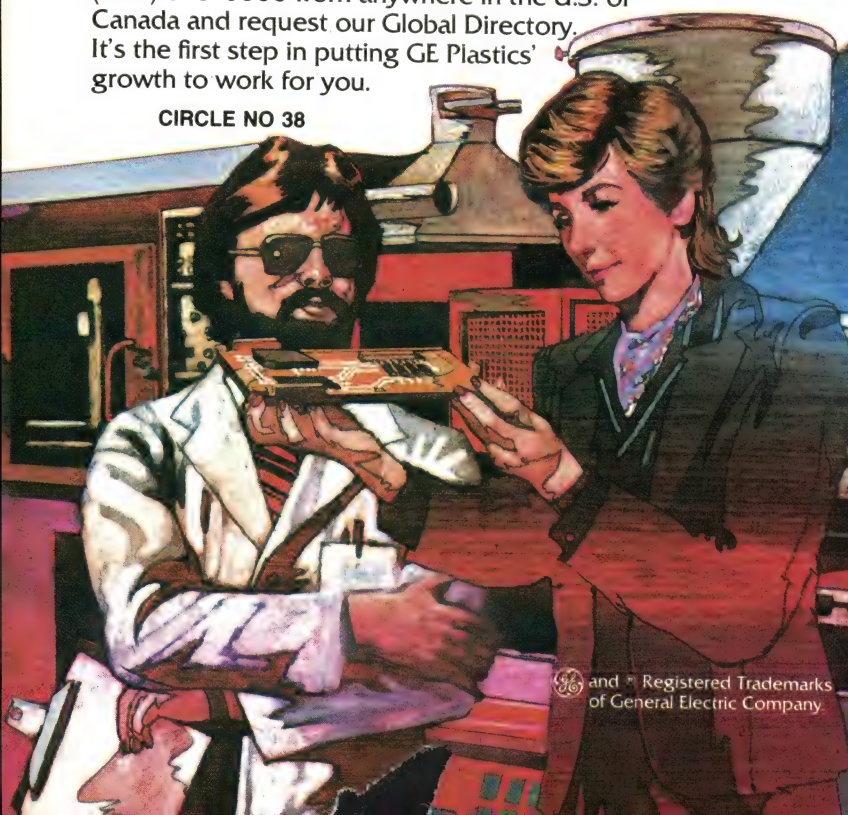
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disk memory more than would a screen editor. This fact explains why apparently similar machines are rated for different numbers of users by the manufacturers. Motorola, for instance, rates its system for four users. Other manufacturers with comparable systems rate their machines for many more users. The

explanation is that Motorola assumes users will be doing computationally intensive tasks like compiling programs, whereas the other manufacturers assume less strenuous use of their machines' facilities.

Beginning a software-development project with one of these systems involves no more effort than

unpacking the system, plugging it in, and configuring the system for your terminal (assuming you know how to start up a complex operating system without crashing it). Indeed, using an OEM computer system could be the optimal strategy for your 32-bit project, because you may not want to expend any effort

TABLE 1—REPRESENTATIVE OEM TARGET/DEVELOPMENT SYSTEMS

COMPANY	MODEL	OPERATING SYSTEM	μ P	BUS	STORAGE (BYTES)			USERS	PRICE		COMMENTS
					RAM	HARD	FLOPPY		LOW	HIGH	
CIE SYSTEMS	680	UNIX, REGULUS, RM/COS	68000	MULTIBUS	256k TO 1M	10M TO 300M					
CYB SYSTEMS	DATAMASTER	UNIPLUS+, UNIX V	68010	MULTIBUS	3.5M TO 12M	334M TO 1.2G	1M	16 TO 32	\$28,995	\$60,000	ETHERNET STD IBM PC SOFTWARE INTERFACE AVAILABLE
DIGITAL EQUIPMENT CORP	MICROVAX II	VMS, UNIX		Q BUS	2M TO 5M	31M TO 456M	800k 95M (TAPE)	1 TO 24	\$20,840	\$76,135	ADA, EXTENSIVE SOFTWARE-DEVELOPMENT TOOLS, ETHERNET, FLOATING-POINT PROCESSOR, BIT-MAPPED DISPLAY AVAILABLE
DY-4 SYSTEMS	DSMO6816	UNIX	68000/10	VME BUS	1M	40M	1M		\$16,570		
FORCE COMPUTERS	MICROFORCE-1 MICROFORCE-2	UNIX V, PDOS, COHERENT	68010	VME BUS	1M TO 2M	25M TO 85M	1M 1M	2	\$5995	\$14,000	RTK REAL-TIME KERNEL
GIMIX	GMX68020	UNIFLEX	68020		2M	19M TO 85M	2M	39	\$13,680	\$17,180	INTELLIGENT I/O BOARDS, LISP, PROLOG, FORTH, ADA
HEURIKON	MINIBOX 814/68010	UNIPLUS+, UNIX, CP/M-68k, VRTX, C-EXEC	68000/10	MULTIBUS	128k TO 1M	30M TO 280M	1M	16	\$11,900	\$14,700	ETHERNET, ADA, APL
IRONICS	IV-1600/D	UNIX V, CP/M-68k, PSOS	68010	VME BUS	1M	10M TO 80M	640k	16	\$12,000		ADA
MOTOROLA MICROSYSTEMS OPERATION	VME SYSTEM 1131	UNIX V, VERSADOS (REAL TIME)	68020	VME BUS	2M TO 10M	70M	655k	4 TO 10	\$14,995	\$30,000	IN-CIRCUIT EMULATOR SUPPORT
NATIONAL SEMICONDUCTOR	VR32	UNIX V	32016	MULTIBUS	1M TO 10M	40M	1M (20M TAPE)	2	\$14,450		IN-CIRCUIT EMULATOR SUPPORT, REAL-TIME KERNEL, I/O DRIVER SOURCE PROVIDED
OMNIBYTE	OB68K/SYSII	IDRIS, UNIX, POLYFORTH, CEEXEC, VRTX, MTOS/68k	68000/10	MULTIBUS	512k	20M TO 80M	1.2M TO 1.6M		\$11,845	\$27,595	
PACIFIC MICROCOMPUTERS	PM200	UNIX	68000/10	MULTIBUS	2M TO 4M	20M TO 80M	1M	10 TO 18	\$12,500		
SBE	SBE200 SBE250 SBE300 SBE350	REGULUS, CP/M-68k, POLYFORTH	68000/10	MULTIBUS	512k	20M TO 140M	370k	2	\$5600	\$7300	HARDWARE FLOATING POINT
WICAT SYSTEMS	SYSTEM 150	UNIPLUS+, WMCS	68000	MULTIBUS	512k	10M TO 39M	630k	2			
ZENDEX	194/86	IRMX-86 CP/M-86	80186	MULTIBUS	512k TO 1M	10M TO 40M	1M	4	\$6500		

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Combining the abilities to run Unix-based software-development tools and to accommodate in-circuit emulators, National Semiconductor's \$14,500 VR32 is in reality an OEM computer composed of available board-level products.

at all on hardware design. With software-development time and costs consuming an increasingly larger share of R&D budgets, the potential savings accruing from designing your own hardware may not offset the cost of such development or the cost of delaying the software-development effort until the hardware is ready.

In addition to changing the priorities of hardware engineers, the recent emergence of these powerful target systems mandates a difference in the way software engineers must think, too. It's a distressing fact of life for software engineers that the basic principles of their discipline rest not on fundamental physical laws, but on the shifting state of the computing art. Civil engineers, by contrast, enjoy a much more stable foundation. The angle of repose of a pile of sand hasn't changed one degree since the first civil engineers erected the pyramids or dug the canals of Mesopotamia. Not so with the fundamentals of software engineering. If the hardware changes, so do the principles of software development.

Precepts follow technology

In the past, software engineers developing code for μ P-based products had to contend with an inherently limited computing engine and user interface in the target system.

Other than crude code patches, software development simply couldn't be done on the target system. A microwave oven controlled by a 4-bit μ P does not provide enough inputs or computing power to write programs, for example. Therefore, software engineers had to turn to minicomputers for multiuser development. What began as making the best of a bad situation grew into an article of faith: Big software projects demand big hardware.

The advent of 16- and 32-bit processors changes this style of thinking. Although 4- and 8-bit development won't disappear, increasing numbers of products will be based on the more powerful μ Ps. These products will essentially incorporate powerful general-purpose computers—ie, no big hardware, just more computing power. Although it's unlikely that the hardware and software requirements of a given target system would be exactly those of a corresponding software-development system, if the target system must have the power and flexibility to meet a range of customer needs, then that target system's range can probably accommodate a software-development environment.

For the software engineer who

has been programming on a small, single-user computer like a μ P development system or a personal computer, moving up to a high-performance OEM target system will be a pleasing adventure as he masters a new panoply of software tools. And even though he has gained high-level software tools, he won't have lost the close contact with the target hardware that he's enjoyed with smaller systems in the past.

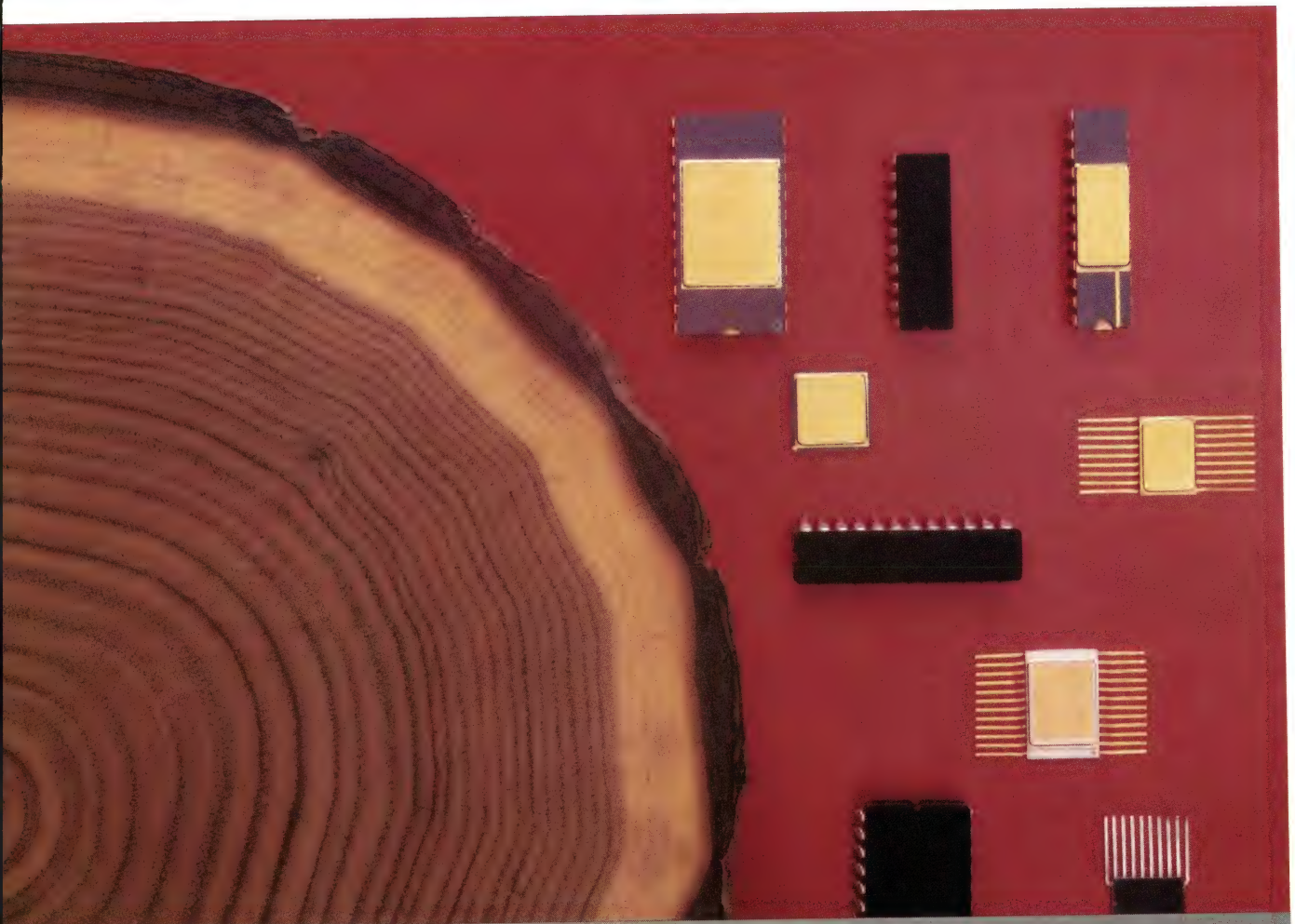
At the other end of the spectrum, the software engineer who's used to working on a superminicomputer need not consider working directly on an example of the target system as a step down. For the most part, the software environment will seem reassuringly familiar.

Furthermore, working directly on an example of the target system can effect a fundamental change in the way the former supermini user works. Downloading code from a supermini host to a target system is enough of a chore that supermini users tend to download and try out relatively large sections of their programs at one time. Working directly on an example of the target system eliminates the downloading step, and software engineers are

This syntax-checking editor from Digital Equipment Corp is an example of the sophisticated software-development tools that you can run on the latest generation of high-performance μ P-based systems.

```
%CC-W-MERGED, Merged "<" and "=" to form "<=".  
12:          if (n<=1)  
%CC-W-SEMICOLONADDED, Semicolon added at the end of the  
              previous source line.  
13:          else  
%CC-E-NOTDECL, "m" is not declared within the scope  
              of this usage.  
15:          return m * factorial (n - 1);  
Buffer $REVIEW          Insert          Forward  
int factorial (n)  
{  
  if (n<=1)  
    return 1  
  else  
    return m * factorial (n - 1);  
}  
Buffer TEST1.C          Insert          Forward  
Keep the indicated correction [Y or N]? 
```


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thus more likely to follow the precepts of recommended software-engineering practice by trying out and debugging individual subroutines, procedures, and modules as they write them.

Networking needs work

In practical terms, the only limitation to using currently available OEM systems for software development is the relatively small number of users who can work on a single system. Where superminicomputers can accommodate 50 or more users, today's OEM systems strain to accommodate more than eight or 16 users.

High-speed networks linking several OEM systems provide an obvious solution to the problem of increasing the number of software engineers working on a project beyond the number that can work on a single OEM computer. Although each manufacturer contacted by EDN reported that such networks will be here very soon, practical networks with robust protection schemes are, in most cases, not quite ready yet. Only DEC claims to

have a networking scheme secure enough to resist tampering by knowledgeable users.

The low cost of these OEM computer systems, however, offsets the limited number of users that they can support. In fact, supporting a small number of users isn't always a limitation. In many cases, you may want to have very small teams—perhaps even consisting of a single software engineer—working on their own computers. For example, in any large project, at least one software engineer will be working on system software. While developing his part of the project, he is very likely to crash the system. If he is working on his own computer, he won't take any of his fellow workers down with him when he does crash.

At the same time, other team members may be working with time-critical code. They will want to connect the computer to logic analyzers, oscilloscopes, in-circuit emulators, and software-performance analyzers to test time-critical code and special-purpose hardware. This task requires direct physical access to the system under test. Testing

this special hardware and software often also involves running special-purpose diagnostic software. These hardware-intensive activities can disrupt the work of users who just want to edit and compile files.

There's one small catch

Perhaps the biggest barrier to "going native" will be management's attempts to recover costs sunk into superminicomputers. Having been talked—some quite recently—into spending hundreds of thousands of dollars for a supermini-computer, management may expect software engineers to use the supermini through its full lifetime, whether or not a less-expensive, multiuser software-development/target system makes sense. As a consequence, some engineers may miss out on a useful innovation.

EDN

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For more information . . .

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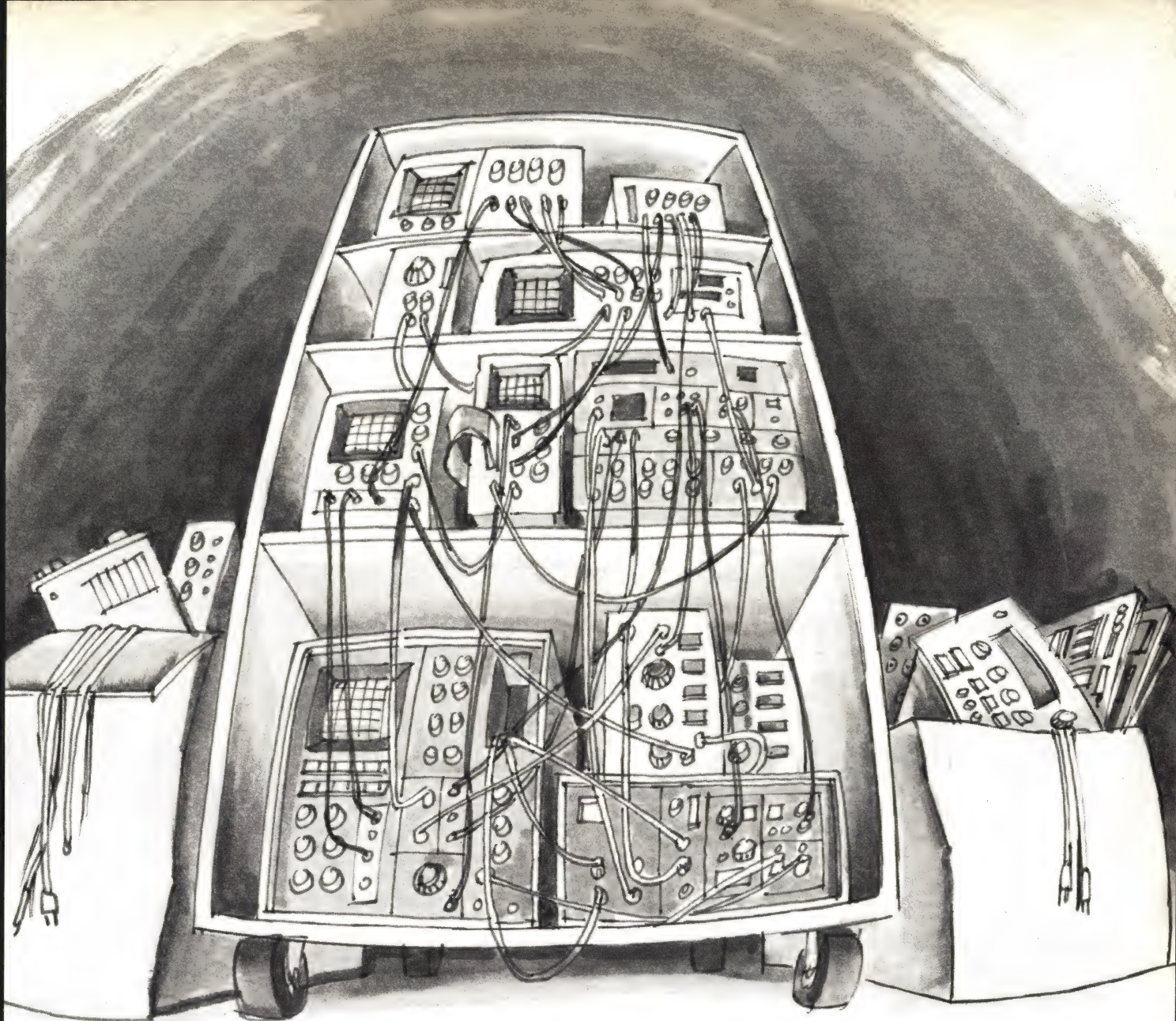
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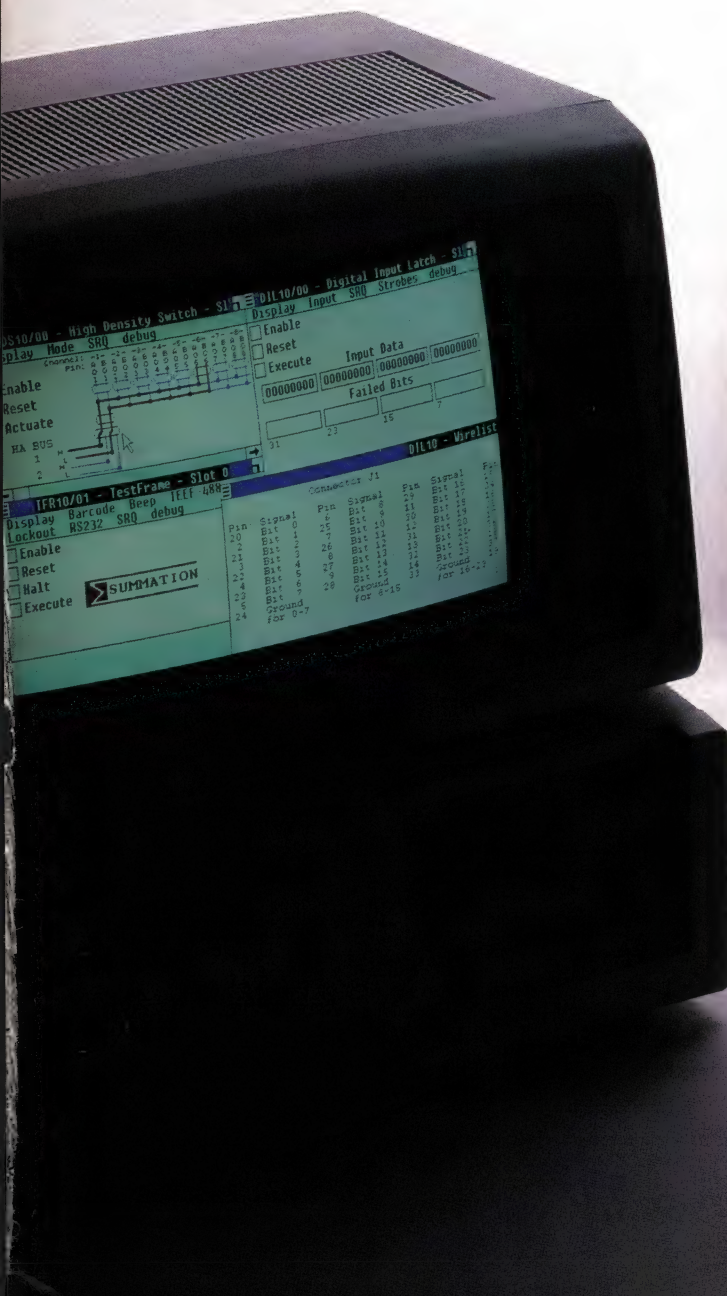
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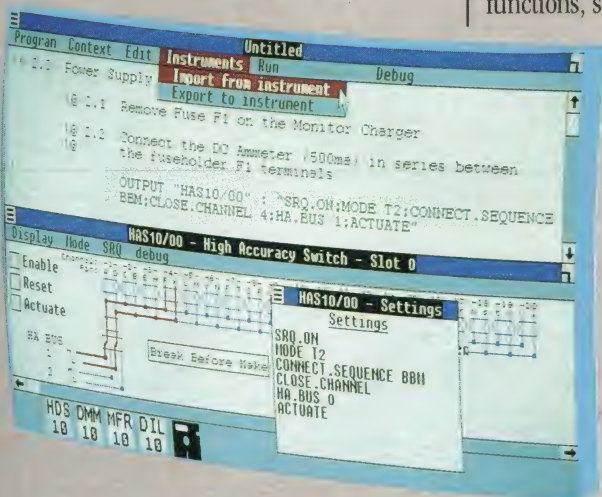
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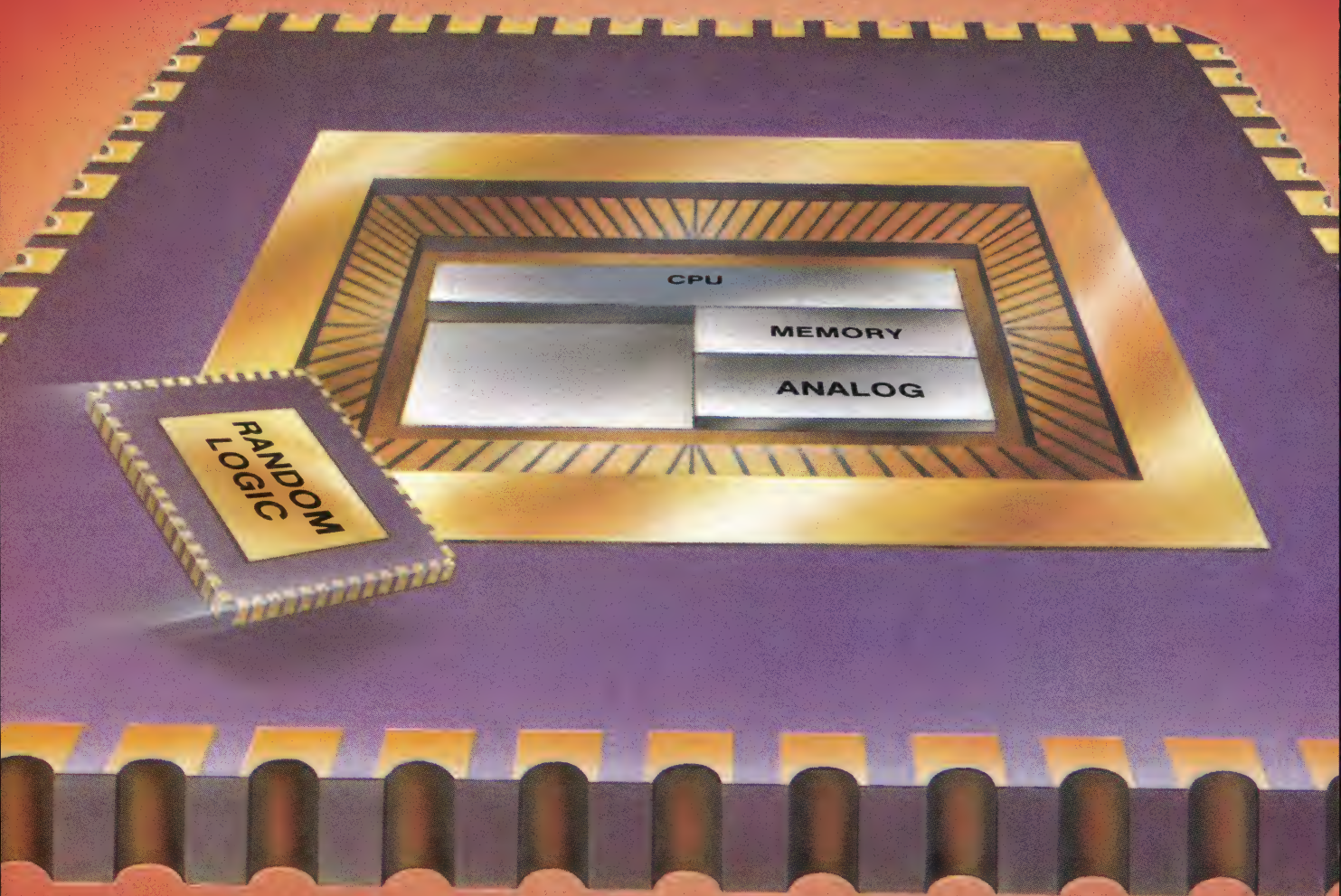
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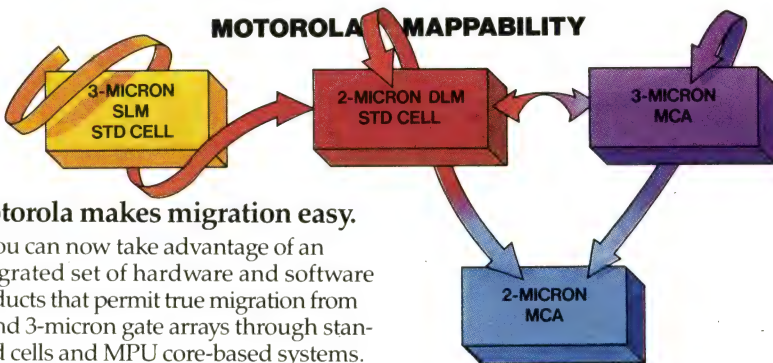
The agreement also covers co-development and alternate sourcing of industry-leading standard cells like the 68HC05 core microprocessor and Motorola's HCA6000 Series HCMOS Macrocell Arrays. Enhanced design flexibility through rapidly expanding libraries driven by the most advanced software is the key to turning your design ideas into reality.

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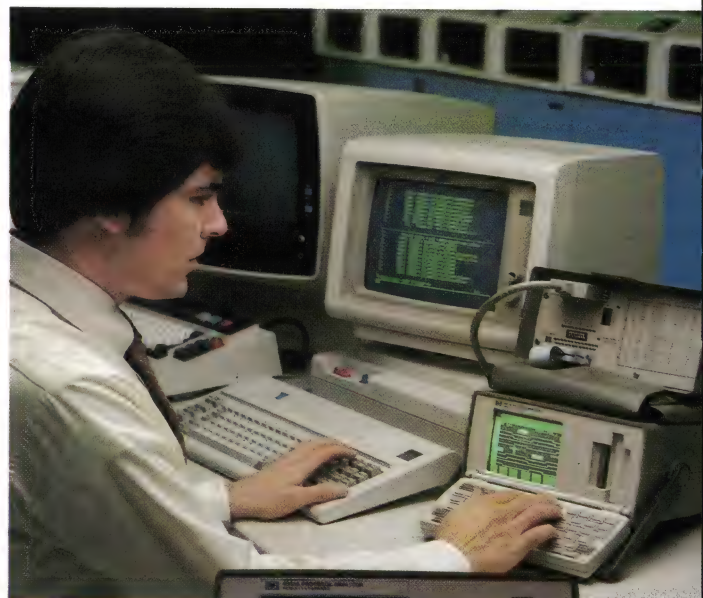
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Electromechanical, solid-state devices satisfy radio-frequency switching needs

Tom Ormond, *Senior Editor*

Because coaxial (or RF) switching is a mature technology area, recent product introductions reflect no startling technological breakthroughs. Instead, switch designers are working to improve the reliability of their products and are successfully increasing the upper frequency limit of coaxial switches. Electromechanical coaxial switches can now operate to 26.5 GHz, and investigation of new connector designs promises to push this switching limit to about 40 GHz. In addition, some manufacturers are employing design techniques to improve reliability without exacting size penalties.

Working in a vacuum

One such concept employs a design that houses the relay-switch contacts in a vacuum. High dielectric strength is the major advantage of such a technique. As a rule of thumb, a vacuum device has a dielectric strength of 1000V per mil. Consequently, relay-contact separation can be quite small and still withstand high voltages. Limited contact movement minimizes relay size; it also permits the use of small, simple actuating mechanisms, and it improves switching times.

Use of a vacuum as a contact environment also improves operating reliability and relay lifetime. The lack of oxygen prevents contact corrosion and the formation of oxides and organic materials that can increase circuit resistance. Because contact resistance is low and stable, circuit losses are low. RF insertion losses typically range between 0.02 and 0.1 dB over the operating-frequency range.

The insertion-loss parameter

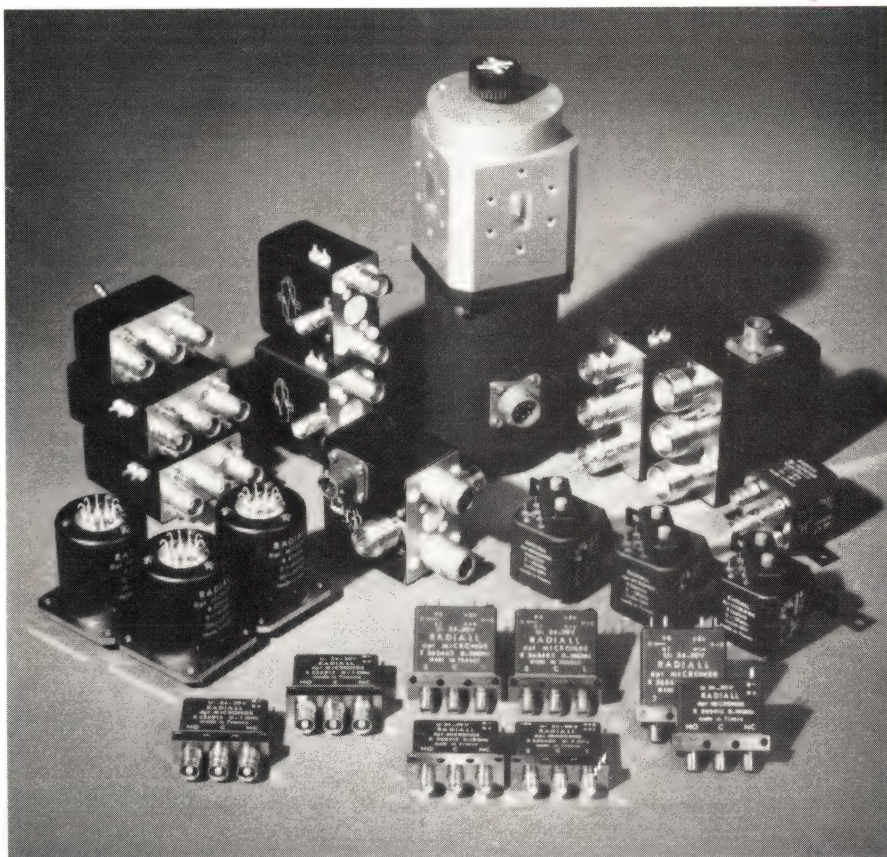
serves as one of the key criteria when it comes to specifying a switch for your system. With coaxial switches, selection is heavily dependent upon application. For example, if switching speed is the primary design concern (as in a phased-array radar application), then your best bet is a solid-state (PIN-diode) switch. On the other hand, if insertion-loss figures are critical (as they are in satellite communication links), then an electromechanical switch proves best.

Although switching speed and insertion loss are the two key parameters that govern the match between a switch and an application, you

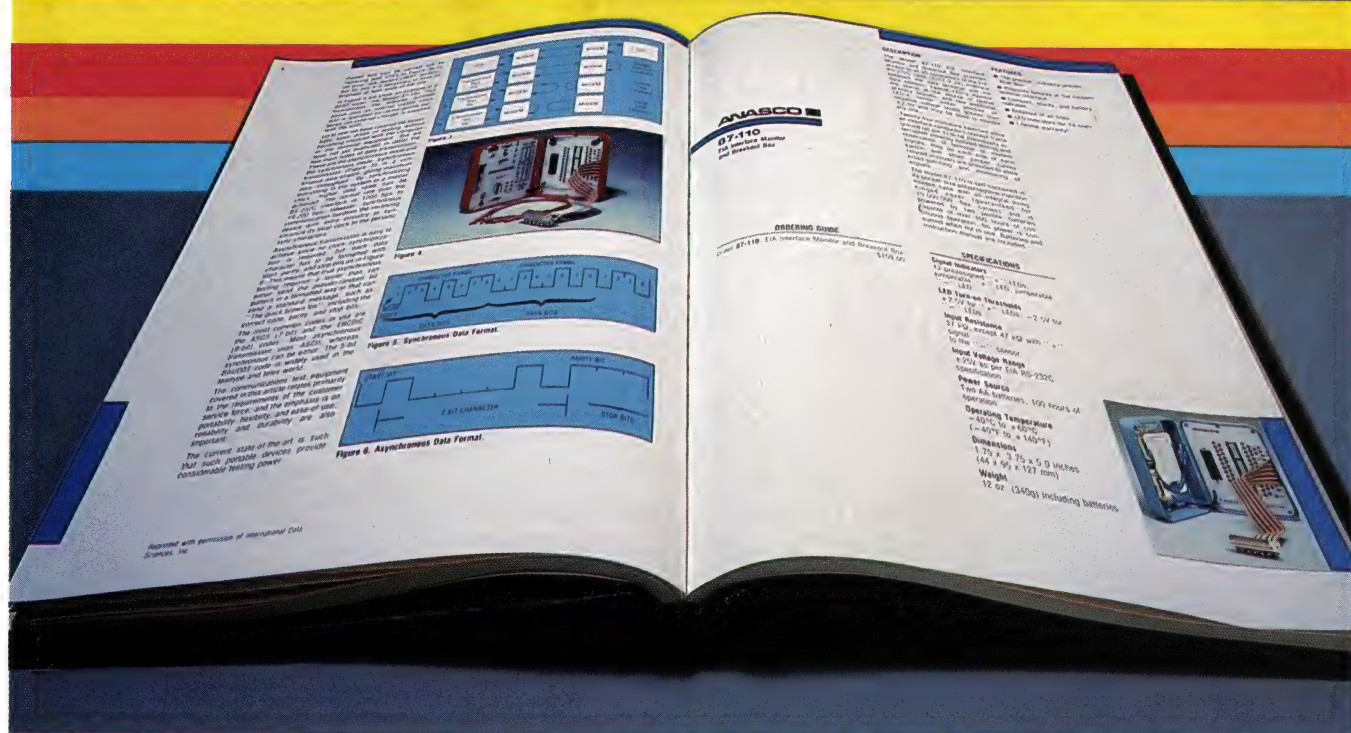
should be aware of some other differences between electromechanical and solid-state switches. Because of their inherent size advantage, PIN-diode switches lend themselves to integration into pc-board circuits that employ microwave strip-line technology. On the negative side, PIN-diode switches can't handle high levels of RF power, and they need to be constantly biased to maintain an on condition. Insertion-loss figures are also relatively high.

In contrast, electromechanical switches have better insertion-loss figures, and they can handle higher RF-power levels. In addition, they are available in latching-type ver-

Housed in packages that meet military specs, F-TEC's spdt to sp6t electromechanical switches operate over -55 to +85°C and feature a 20-msec switching time.



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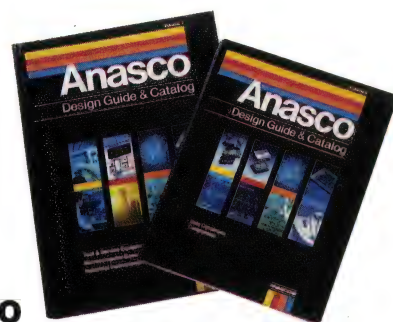
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sions (units that can be actuated with a pulse rather than a constant bias level), so they typically consume less power.

The low-loss solution

You should consider all of the foregoing switch-selection criteria—insertion loss, switching speed, and switch size, as well as power-handling capability and power consumption—and how well they match your application as you evaluate the recent offerings from coaxial-switch manufacturers.

For high-switching-speed, hostile applications, for example, F-TEC offers a line of miniature electromechanical switches that can accommodate a 26.5-GHz frequency. Housed in a rugged, high-reliability package that meets MIL-C-3928, they are available in both multiposition (spdt to sp6t) and transfer configurations in either latching or failsafe operating modes. All units accommodate dc to 18-GHz frequencies, and the spdt failsafe models handle 26.5 GHz. Standard operating voltage specs at 24 to 30V dc (at currents of 57 to 150 mA at 28V dc); 12V, 48V, and TTL-compatible driver versions are optional.

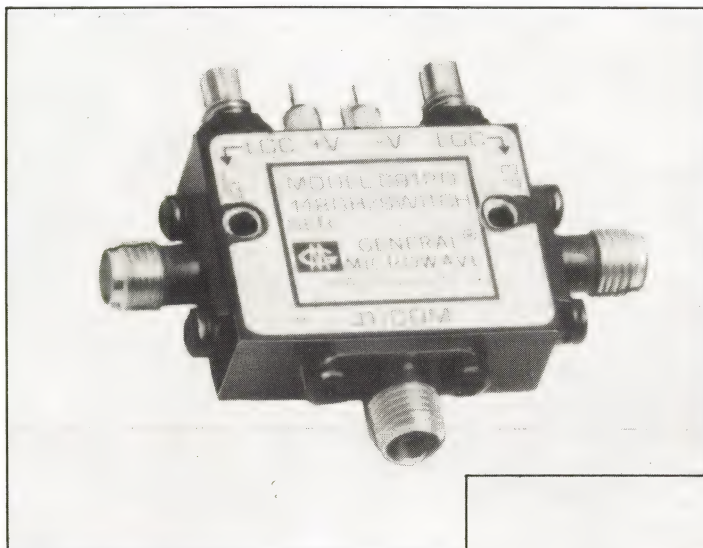
SMA connectors minimize size

The switches operate over -55 to $+85^{\circ}\text{C}$ and spec a 20-msec switching time. They are 100% swept-frequency tested and guaranteed for 1M cycles min. They feature SMA connectors to minimize size and weight, and they are compatible with 50 Ω systems.

Maximum insertion loss for the switches is 0.2 to 0.7 dB, depending on model. Maximum VSWR ranges from 1.25:1 to 1.8:1, and isolation specs at 40 to 70 dB min. Power-handling capability ranges from 100W at 0.1 GHz to 20W at 18 GHz.

Switch specs 25M operations

Another high-reliability electromechanical switch was conceived to switch solid-state transmitters in the US Air Force relocatable over-

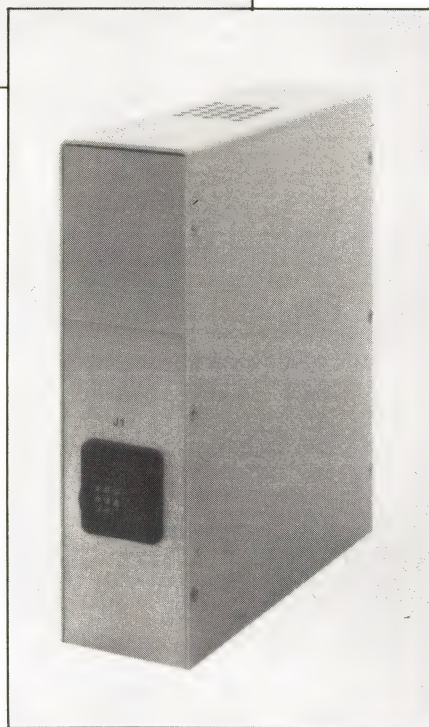


Using an assembly of PIN diodes mounted in a microstrip transmission line, General Microwave's G91 Series switches handle frequency ranges of 1 to 18 GHz.

the-horizon radar (ROTHR). The RC496200H440 vacuum coaxial relay from Jennings is an sp4t device capable of switching a high-power RF transmitter to multiple outputs such as those of filter networks and antennas. Over a 2- to 30-MHz bandwidth, the switch handles 5 kW of RF power. The unit is truly a high-reliability switching device: Estimated switching life specs at 25M operations.

The relay features a copper body with the inner conductors sealed into the ends of the housing by vacuum-tight ceramic-disk insulators. A switch plate, slotted for multiple positive contacts, provides an electrical connection between the inner conductors. A metal bellows on the movable contacts allows movement within the vacuum chamber and maintains the vacuum-tight seal. The actuating mechanism is a bistable device that uses permanent magnets that operate as positive latching devices. A balanced spring provides additional drive power for contact movement and also acts to neutralize atmospheric pressure.

The \$1730 RC496200H440 suits 50 Ω systems. Insertion loss at 30 MHz is 0.05 dB, and maximum VSWR over the operating-fre-



Offering easy module interchangeability via quick-disconnect connectors, the Model 4108 8x8-module coaxial relay switching system from Matrix Systems is self-contained. You need only connect the TTL control signals and dc power through dual card-edge connectors.

cy range is 1.2:1. Switching time, including contact bounce, specs at 20 msec. Minimum isolation is 42 dB at 28 MHz.

The electromechanical switch's nominal control voltage is 26.5V dc; minimum and maximum values are 17.5 and 32V dc, respectively. Dropout voltage specs at 10V dc. An LC-type coaxial-jack receptacle serves as the RF input termination, and control signals are terminated

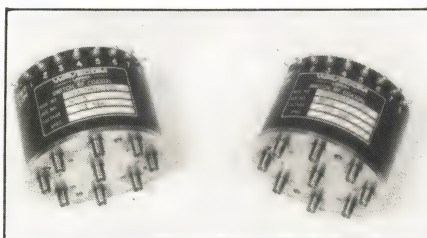
TECHNOLOGY UPDATE

via a 4-position terminal strip. Dielectric withstanding voltage at 60 Hz specs at 4000V peak.

Switches span dc to 18.5 GHz

Another supplier of MIL-standard electromechanical switches is Wavecom, whose sp8t Series 081 offers a switching capability from dc to 18.5 GHz in addition to the company's reliability guarantee of 1M cycles per position without intermittent contacts. The switches spec an insertion-loss increase of less than 0.1 dB. Typical performance specs include VSWR figures from 1.15:1 at 3 GHz to 1.5:1 at 26 GHz. Insertion loss ranges from 0.15 dB at 2 GHz to 0.5 dB max at 26 GHz. Isolation is 100 dB at 2 GHz and 60 dB typ at 26 GHz. Phase mismatch between channels is 0.1 dB from dc to 18 GHz and 0.15 dB from 18 to 26 GHz.

Each Wavecom switch is available with TTL-compatible driver circuitry (or a BCD decoder) that accepts the standard high-level (2.4 to 5V) or low-level (0 to 0.8V) logic signals. Isolated dc-indicator circuitry that accommodates computer monitoring (or visual observation) of switch position/operation is also available. All



Guaranteed for at least 1M cycles, Wavecom's Series 081 sp8t switches spec a 1.5:1 VSWR, a 0.5-dB insertion loss, and 60-dB typ isolation at 26 GHz.

latching configurations are available with de-energizing (power-breaker) circuitry that prevents control-circuit power dissipation. The switches include optical devices that isolate computer signals from the main power supply. Features include internal 50 Ω terminations (rated for 5W continuous), isolated indicator circuitry for remote monitoring, and driver circuitry.

The solid-state solution

In contrast to the characteristic low-insertion-loss, high-power-handling capabilities of the foregoing switches, solid-state (PIN-diode) switches can usually offer size and speed advantages over their electromechanical counterparts. Among the manufacturers of such solid-

state switches is General Microwave, which offers single-pole, multithrow switches that cover a 0.2- to 18-GHz frequency range in two bands: Series G92 spans 0.2 to 4 GHz, and Series G91 handles 1 to 18 GHz. The switches, available in spdt through sp7t configurations in both reflective and nonreflective modes, meet military requirements for humidity, shock, vibration, altitude, and temperature cycling.

Switches based on PIN diodes

All of the G91 and G92 units operate from one supply (5 to 15V at currents ranging from 100 to 190 and 30 to 80 mA, respectively) and include built-in TTL-compatible drivers. The switches are based on an IC assembly of PIN diodes mounted in a microstrip transmission line. The integral drivers provide the currents that switch the ports on and off.

G91 and G92 PIN-diode switches operate over -65 to $+110^{\circ}\text{C}$. Other electrical specs vary as a function of model. Switching times, for example, range from 75 to 200 nsec. Isolation ranges between 40 and 60 dB min, and insertion loss is 1.2 to 3.8 dB max. VSWR figures span 1.5:1 to 2.3:1 max. Reflective versions can handle 1W loads, and nonreflective units switch 100 mW. Prices start at \$450.

Capable of handling 5 kW of RF power over 2 to 30 MHz, ITT Jennings' vacuum-style coaxial switches suit 50 Ω systems. They spec a 0.05-dB insertion loss at 30 MHz and a 20-msec switching time.



Switches span 10 to 2500 MHz

Another supplier of PIN-diode coaxial switches is Mini-Circuits Laboratory, whose line includes both spst (Model PSW-1111) and spdt (Model PSW-1211) designs. Both versions operate over 10 to 2500 MHz; insertion losses are 1.1 to 1.7 dB from 10 to 1250 MHz and 1.7 to 2.7 dB from 1250 to 2500 MHz.

Minimum isolation figures vary as a function of operating frequency and measure 40, 30, 25, and 20 dB over 10 to 500 MHz, 500 to 1000 MHz, 1000 to 2000 MHz, and 2000 to 2500 MHz, respectively. On-state VSWR is 1.5:1 max, and switching speed specs at 1 μsec max. The

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switches operate from 5V dc (at 5 mA max), and the RF signal ports accommodate 20-dBm inputs max. Operating range spans -54 to +100°C. Both models cost \$29.95.

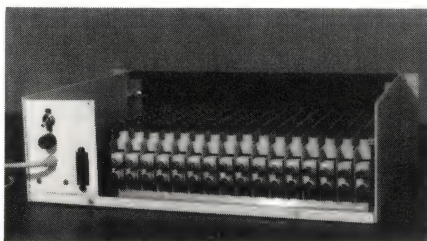
Switch systems save design time

Unlike the foregoing preassembled switches, Cytec's Series CX programmable coaxial switching systems consist of switching modules, latching modules, and mother boards that you can assemble into any matrix or multiplexer configuration. The computer-controlled systems include a front-panel display that provides relay and status feedback to the computer.

The switching modules use reed switches placed on pc boards via strip-line technology to achieve a 50Ω characteristic impedance. The switches have a flat (within 1 dB) frequency response from dc to 400 MHz.

Modules use BNC receptacles

Two types of switch modules are available. The CX8A module has eight BNC receptacles on one side of the relays switched to two BNC receptacles on the bus side of the relays. CX8B modules have two BNC receptacles on the bus side of the relays; on the input side, the



Using reed relays as the switching element, Cytec's Series CX programmable coaxial switching systems consist of switching modules, latching modules, and mother boards.

eight relays are wired to a card-edge connector that plugs into a coaxial mother board.

A CL8 display module is required for each switch module. Each module includes control logic for selecting a relay and eight LEDs for reporting status and indicating energized relays.

CX Series mainframes are available as single-chassis units or as expandable systems with one control mainframe and several expansion chassis. Each mainframe is supplied in a 19-in. rack-mountable housing and is prewired to accept switching modules, control-I/O modules, and display modules.

Two mainframe types are available. Series A units use CX8A switch modules and are available in configurations that control eight or 16 switch modules. Series B main-

frames use the CX8B switch modules and are prewired in a matrix configuration—either 8×8 or 16×8 modules.

Optional control modules

Plug-in control modules are optional. They are compatible with 16-bit parallel-I/O, IEEE-488, or RS-232C serial interfaces. Optional manual controls allow you to select relays from the mainframe's front panel.

Finally, capitalizing on the space savings that solid-state switches can provide, Matrix Systems offers its Model 4108, an 8×8-module wideband coaxial relay matrix that measures 6×7.2×2.2 in.; the unit thus occupies about 40% of the space required by competitive devices. The stand-alone switch, which operates over dc to 500 MHz, features decoding and latching circuitry with interlock to prevent input shorting.

The 4108 suits wideband test and IF systems as well as high-resolution video, fast-rise ECL, and VHF/UHF cable-TV systems. Insertion loss over the entire frequency range specs at 1.5 dB max, and isolation measures 56 dB min. Relay contacts are rated at 28V dc and 500 mA (3W max); contact resistance measures 400 mΩ.

The module requires you to supply only TTL control signals and dc power (5V at 2.5A) through dual card-edge connectors. Signal interface is through two 8-pin quick-disconnect coaxial connectors. Status feedback allows you to verify switch-point closures through the control bus.

The control logic is interlocked internally. Because the module is both bidirectional in its signal path and reversible in card-edge connector configuration, you can interlock either the input or the output. The 4108 costs \$3200. **EDN**

For more information . . .

For more information on the coaxial switches described in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

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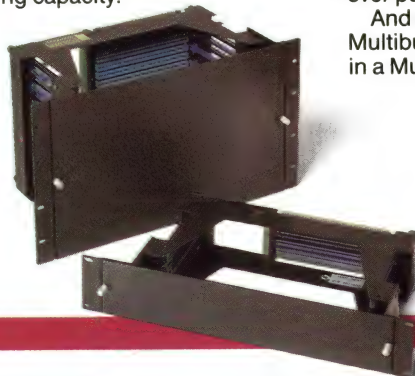
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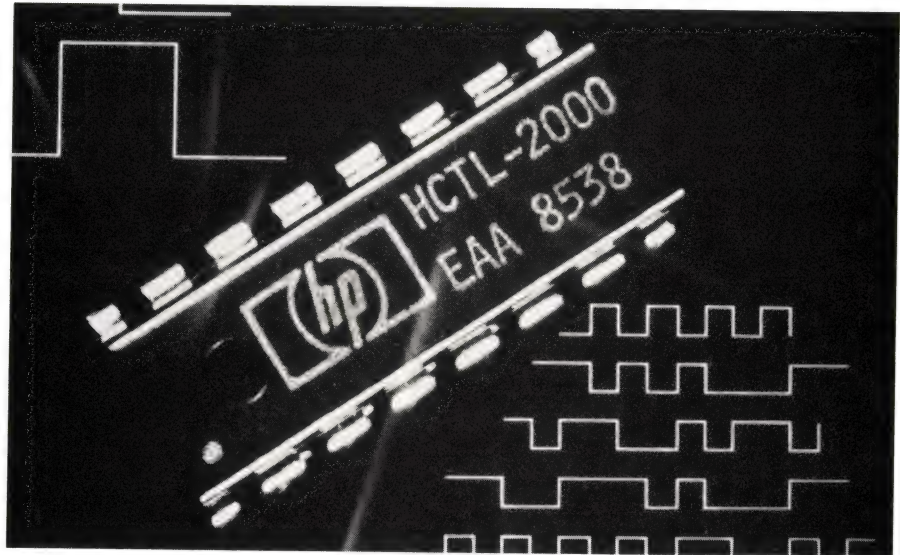
Motion-control and quadrature-decoder ICs eliminate or relieve host microprocessors

Two motion-control ICs reduce component count in digital motor-control systems. The simpler of the two, Model HCTL-2000, is a quadrature-decoder and counter-interface device. The other, Model HCTL-1000, is a dedicated microprocessor that performs all motion-control functions required in high-performance servo loops. Fabricated in a CMOS process, the -2000 comes in a 16-pin single DIP; the NMOS-based -1000 occupies a 40-pin double DIP.

Model HCTL-2000 accepts digitally encoded quadrature signals from an optical shaft encoder or a digital potentiometer and converts the signals into μ P-compatible signals. The unit contains a digital input-noise filter; a quadrature decoder; a 12-bit binary counter with latched outputs; a multiplexed, 8-bit parallel-output port; and an interface-control logic section.

Using the quadrature signals from the encoder or potentiometer, the -2000 maintains a 12-bit count value that reflects the shaft position of the encoding device. The system's host μ P can sample this count value periodically and integrate the data into a multibyte representation. An 8-bit data mode is available for applications not requiring a 12-bit count value. For asynchronous data, a latching and interface control prevents data from changing between two byte-read operations.

The HCTL-1000 provides position and velocity control to motors by comparing the command position from the host processor with the actual position feedback from an incremental encoder. An 8-bit, multiplexed bidirectional address/data bus provides the interface to the host processor. The IC decodes the encoder feedback into quadrature



Designed for closed-loop, motion-control systems, the HCTL-2000 quadrature-decoder and counter-interface IC reduces system software and relieves the system's μ P of time-intensive quadrature-decoding functions.

counts; a 24-bit counter keeps track of position.

The chip's preprogrammed ROM and dedicated ALU allow you to choose any one of four control algorithms to suit your particular application. The four control modes are position control; proportional velocity control; automatic trapezoidal profiling for point profiling using linear acceleration; and integral velocity control with continuous velocity profiling.

A programmable digital filter aids in the computation of the compensated motor command. This computed output is available to external amplifiers either as an 8-bit byte or as a pulse-width-modulated signal. The HCTL-1000 can provide electronic commutation for brushless-dc and stepper motors. Encoder-generated position information ensures that motor phases occur in the correct sequence.

The commutator is fully programmable, and it suits most motor/encoder combinations. In addition, you

can program the commutator for phase overlap and phase advance to reduce torque ripple and improve high-speed response. The -1000 works as a digital sampled-data system. Although the IC accepts information from the host processor on an asynchronous basis (with respect to the control functions), it computes motor commands on a discrete sample-time basis. With a 2-MHz external clock, the part has a sampling time that can vary from 64 μ sec to 2 msec.

The CMOS HCTL-2000 operates over -40 to $+85^{\circ}\text{C}$, and the NMOS HCTL-1000 operates over 0 to 70°C . Both devices work from one $5\text{V} \pm 5\%$ supply. The CMOS part dissipates 300 μW typ; the NMOS device consumes 400 mW typ, 950 mW max. The HCTL-2000 and -1000 cost \$8.50 (100) and \$28.25 (250), respectively.—**Bill Travis**

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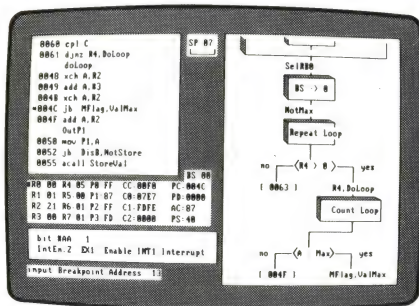
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8051

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8088

8085

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CIRCLE NO 50

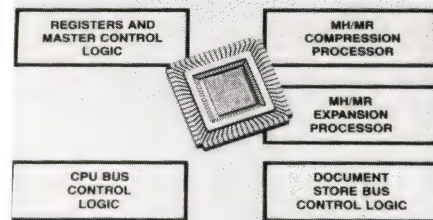
PRODUCT UPDATE

Compression/expansion chip compresses text by 30:1 ratio

The single-chip Am7970 compression/expansion processor permits text-file compression ratios of 30:1 for use with document-processing equipment, such as laser printers, copiers, scanners, and facsimile terminals. The chip compresses and expands 2-tone, bit-mapped image data in accordance with the international T.4 and T.6 CCITT compaction-protocol standards for Groups 3 and 4 facsimile equipment. You can program compression and expansion independently for 1-dimensional Huffman coding; 2-dimensional, modified READ (relative address designate) coding; or transparent data transfers.

If you employ this chip at the pixel level, you can obtain compression ratios as high as 50:1, even at pixel-transmission rates of between 2M and 8M bps. At these rates, the Am7970 can be a general-purpose storage and retrieval compaction device for transferring compressed versions of both text and image data in full-duplex mode. Because of its large compression ratio, the chip greatly reduces the amount of memory space required to retain text or image data on high-volume storage media, such as magnetic tape or video disks.

After initialization, the chip operates via 38 internal control registers and an external interrupt line. The chip's CPU bus-control logic provides an interface to an 8088 μ P. You can program it to handle line lengths or document widths as great as 16k pixels; it yields document resolutions as high as 400 pixels/in. In full-duplex mode, the chip can be programmed for either 1- or 2-dimensional encoding and decoding. For 2-dimensional operation, a programmable K parameter defines the number of lines for the



Using a dual 24-bit bus architecture, the Am7970 compression/expansion processor compacts data into a variety of formats either to reduce storage space or to increase effective transmission rates.

coding sequence. By setting the K parameter to infinity (ie, by setting all three bits equal to zero), you can use the Group 4 error-correction protocol with maximum compression.

The chip offers other compaction modes as well. For instance, in the Express Mode, the chip compresses only every Nth line (where N=1 to 255); in the Expander Granularity Mode, the IC repeats each line one to seven times. You can determine top, left, and right margins and specify windowing.

In addition to the system address-data bus, the Am7970 has a local document-store address-data bus, so it can address a total of 32M bytes of linear-address space. Starting addresses, buffer lengths, and current addresses for raw and processed data are stored within independent on-chip registers for both compressor and expander functions, respectively.

Operating from a single 5V supply, the 7970 dissipates 1.5W typ over 0 to 70°C. The part is housed in either a 68-pin leadless chip carrier (LCC) or a pin-grid array, and it costs \$245 (100). —Denny Cormier
Advanced Micro Devices, Box 3453, Sunnyvale, CA 94088. Phone (408) 982-7445.

Circle No 726



**Stop
Oscillator**

Street-wise designers: use the ultimate in speed and power control.

New Harris 82C85 Static Clock Controller operates in four low-power modes.

The new Harris 82C85 static CMOS clock controller/generator dramatically reduces power consumption in static CMOS systems by giving you four distinct operating modes.

- Full Speed for top performance.
- Slow mode for low power and continuous operation.
- Stop Clock for low power and instant restart.
- Stop Oscillator for minimum power standby operation.

Designed specifically for 80C86 and 80C88-based systems, the 82C85 responds to a software HALT command, stopping all system clocks automatically. The 82C85 can also be controlled by a flexible independent START and STOP control structure.

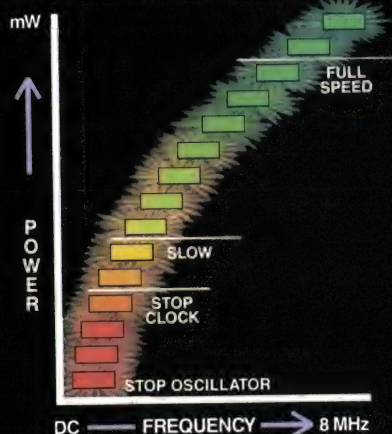
With a full DC-8MHz operating frequency range, the 82C85 allows you to control your system power and performance, tailoring them to your exact requirements.

Stop...With no loss of data! Accelerate...With no delay!

It's the control you've been waiting for — for your portable instrumentation, industrial process control or military guidance systems. In fact, it's easy to design into any CMOS system that needs extremely low operating power.

The new Harris 82C85 static CMOS clock controller/generator — the next generation of system control from the world's leader in 16-bit CMOS micro-processors.

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MHS Semiconductor
Sales Ltd., Eskdale
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Wokingham, Berks,
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PRODUCT UPDATE

8-bit single-chip μ C offers EPROM program development

The TMS7742, an 8-bit single-chip microcomputer, incorporates a 4k-byte on-chip EPROM to facilitate prototyping and development. For low-volume projects, this μ C can be a cost-effective alternative to masked-ROM devices. The chip is also useful in designs that include program parameters that are subject to frequent changes.

The chip puts a standard 2732 EPROM design into the silicon area that would normally contain a masked ROM. To program the TMS7742, you can use a standard PROM programmer and a 40- to 24-pin adapter socket with the RESET and XTAL2 pins grounded.

In addition to its 4k-byte EPROM, the TMS7742 has 256 bytes of RAM, a serial-I/O port, two 13-bit timers, and one 10-bit timer that you can use as a baud-rate generator. To reduce software overhead and shorten the interrupt-response time, the chip's register-to-register architecture lets you use the RAM locations as registers.

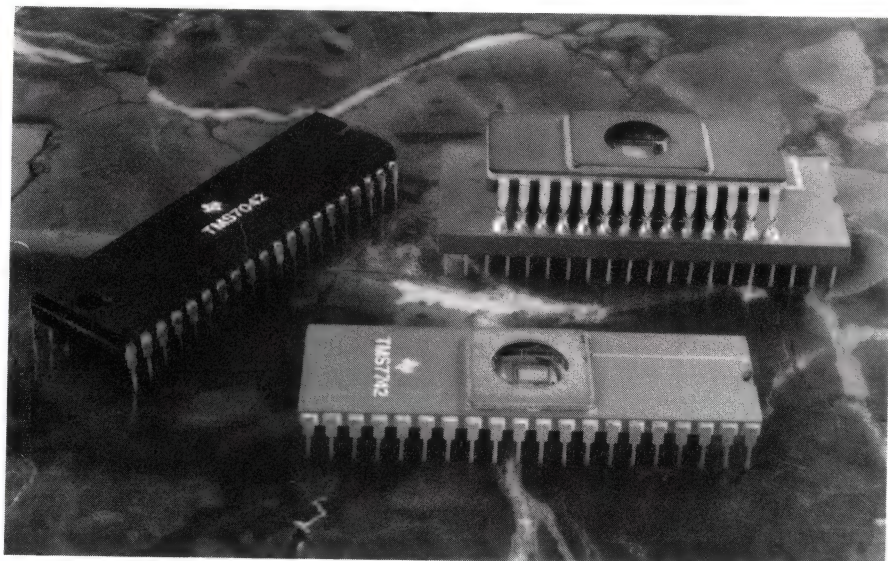
Consequently, this chip doesn't require an accumulator for direct-register arithmetic and logical operation. Clock frequency ranges from 1 to 5 MHz.

The TMS7742 has 32 TTL-compatible I/O pins: 22 bidirectional pins, eight output pins, and two input pins. Using Intel or Motorola multiprocessor communication formats, the chip's serial port can communicate with multiple devices in asynchronous, isosynchronous, or serial-I/O mode. The serial port operates at a maximum baud rate of 625k bps in the isosynchronous or serial-I/O modes and 78k bps in the asynchronous mode.

Housed in a 40-pin ceramic side-brazed package, the TMS7742 dissipates an average of 900 mW and operates over 0 to 70°C. \$38.40 (100).—**J D Mosley**

Texas Instruments Inc, Semiconductor Group (SC-517), Box 809066, Dallas, TX 75380. Phone (800) 232-3200.

Circle No 727

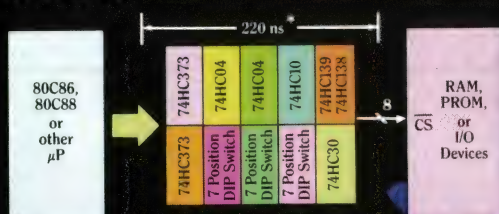


An on-chip EPROM in the TMS7742 8-bit microcomputer gives you programming flexibility in low-volume applications. A ROM version, the TMS7042, is available in a DIP or with a piggyback socket for a 28-pin EPROM.

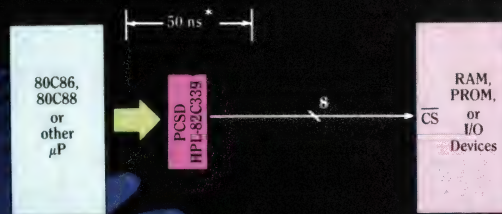
Our new Programmable Chip Select Decoders let you pass up 74HCXX logic.

New Harris HPL-82C339 lets your micros talk directly to peripherals — and it's faster!

BEFORE



AFTER



Harris introduces the industry's first application-specific Programmable Chip Select Decoder (PCSD™) family.

These CMOS devices provide a simpler interface between any microprocessor and its peripherals, offering low power consumption and bipolar speed. In a typical application, they can replace up to seven 74HCXX logic parts — and perform four times as fast!

Decoder architecture options and programmability let you determine which decoding configuration best fits your needs:

- HPL-82C339 (24 pin slimline)
- HPL-82C338 (20 pin)
- HPL-82C139 (16 pin)
- HPL-82C138 (16 pin)

You save board real estate, reduce parts count, improve reliability, and save on your total system cost.

They're perfect for portable PCs, handheld communications equipment and military systems requiring highest performance and lowest power. They're TTL and CMOS compatible, and can be programmed in the factory or in the field.

For full details, contact Harris/MHS Semiconductor Sales Ltd., Eskdale Road, Winnersh, Wokingham, Berks, RG11 5TR, England.

 **HARRIS**

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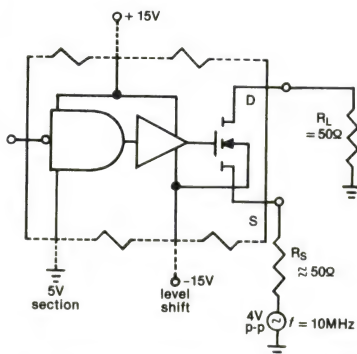
* Speed comparison evaluated using published data sheet specifications at $V_{CC} = 5V \pm 10\%$, $T = -55^\circ C$ to $+125^\circ C$ and $C_L = 50 pF$.

For your information, our name is Harris.

CIRCLE NO 48

D-MOS FET TIP

FET VIDEO SWITCH WITH DRIVER

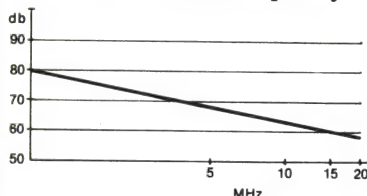


(One channel of a four-channel CDG 309)

More Than 60 db Off Isolation at 10 MHz

D-MOS's low capacitance makes it one of the best high frequency switches around. And when you put it on the same chip with CMOS you have an integrated circuit that can control up to 20 volts p-p... with a 5-volt logic swing.

OFF isolation vs frequency



VCC = $\pm 15V$; $R_L = 50 \text{ Ohms}$;
Vgen = 4V p-p

The CDG family of integrated CMOS/D-MOS switches and drivers offers you many choices—normally-on or -off types, "T" switch configurations, even high interswitch isolation packaging.

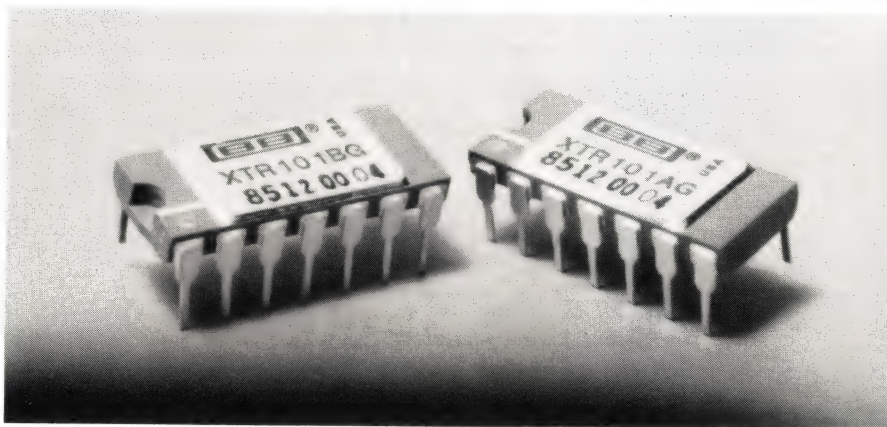
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PRODUCT UPDATE

Current-transmitter circuit uses a single wire pair



Designed to provide data and receive power over the same 2-wire line, the XTR101 4- to 20-mA transmitter supplants the manufacturer's earlier, multichip-hybrid version. The device is ideal for use in noisy industrial environments.

Designed for transmitting sensor-generated and other low-level signals through electrically noisy industrial environments, Model XTR101 4- to 20-mA transmitter transmits data over—and receives its power from—a single wire pair. The 2-wire device performs its function by modulating its power-supply current according to the input-signal source.

The transmitter is immune to voltage drops stemming from long power-supply runs; it also ignores noise from industrial equipment, such as motors, relays, actuators, switches, and transformers. The IC accommodates inputs from a variety of transducers and sensors, such as RTDs, thermistors, and strain-gauge bridges.

The XTR101 contains an input instrumentation amplifier that specs $\pm 0.01\%$ max nonlinearity. The IC also has a voltage-controlled output-current source and two matched 1-mA current sources. The transmitter is housed in a 14-pin metal or ceramic DIP, and it operates over -40 to $+85^\circ\text{C}$. A voltage range of 0 to 1V at the input of the instrumentation amplifier causes

currents of 4 to 20 mA to circulate in the 2-wire output loop.

The XTR101 is a pin-compatible, monolithic version of the manufacturer's hybrid XTR100 2-wire transmitter. Its circuit configuration allows you to use an external output transistor. The use of the external device reduces temperature changes inside the package as the output current changes from 4 to 20 mA. Such temperature changes result in thermal feedback from the output stage to the input stage, and this feedback produces gain nonlinearity.

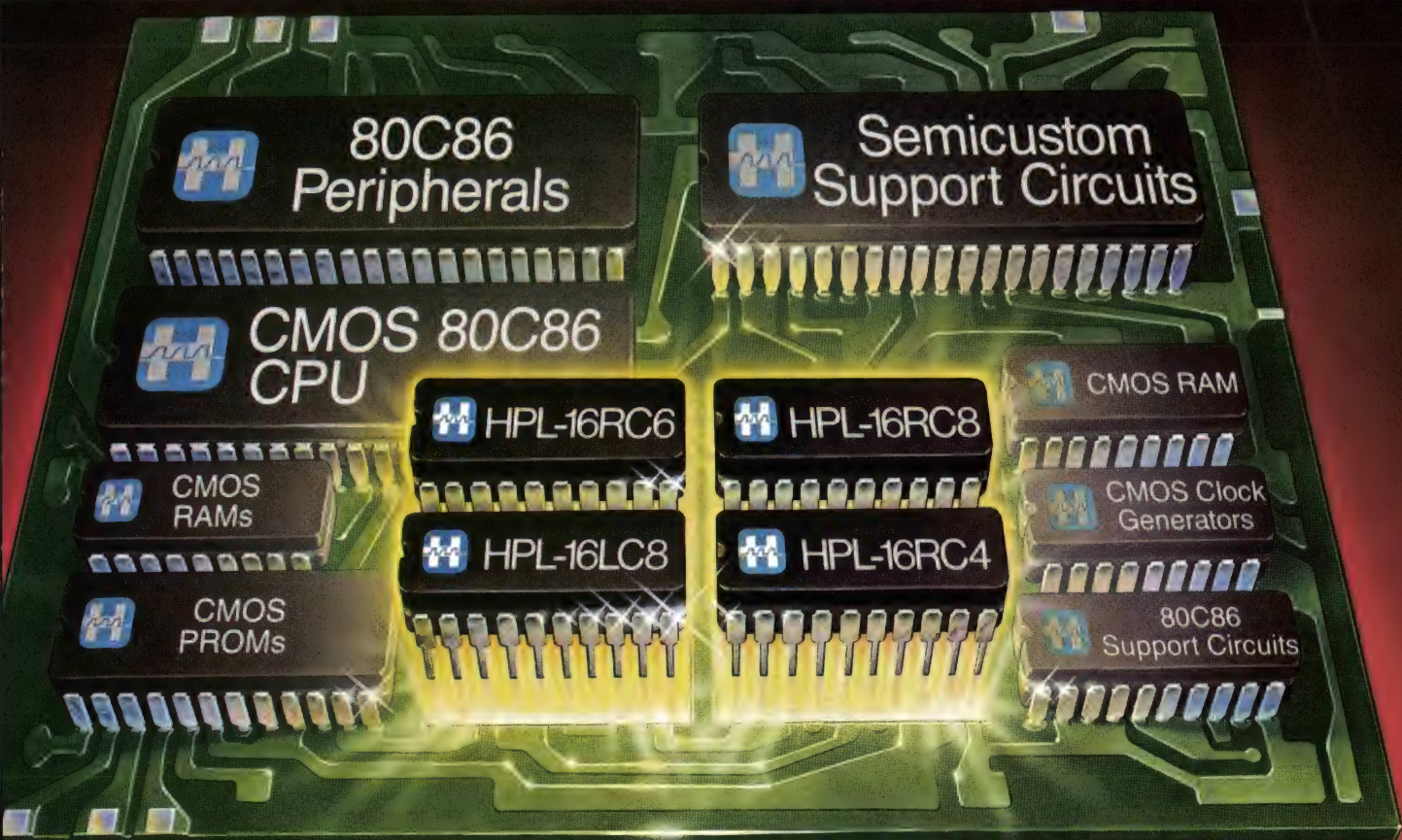
The XTR101 accommodates power-supply voltages from 11.6 to 40V; the power-supply dependency of the internal current sources is typically ± 3 ppm per volt change. Other specs include maximum offset and drift of $\pm 30 \mu\text{V}$ and $\pm 0.75 \mu\text{V}/^\circ\text{C}$, respectively. Common-mode rejection is 90 dB min and bandwidth is 5 kHz min. Price is \$8.25 or \$12.25 (100), depending on grade.

—Bill Travis

Burr-Brown Corp, Box 11400,
Tucson, AZ 85734. Phone (602) 746-
1111. TWX 910-952-1111.

Circle No 728

HARRIS PROGRAMMABLE LOGIC



We've solved the total CMOS system puzzle with a perfect-fitting family of CMOS HPLs™.

Now Harris gives you low-power programmable logic to tie your CMOS system together.

New CMOS HPLs from Harris move your designs to a higher level of integration by replacing multiple SSI/MSI devices with a single logic circuit with on-chip test circuitry.

These static CMOS HPLs are pinout and function-compatible with bipolar HPL/PALs™ yet draw only 5% of the power.

Their cooler operation allows you to shrink board size by eliminating fans and vents, and reducing power supply requirements.

And all HPL products feature VOCAL™ — patented Verification of On-Chip Array Logic — that gives you complete AC/DC and functional testing of blank devices. This can eliminate the need for exhaustive post-programming vector testing.

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Harris CMOS HPLs

Part Number	Pin Configuration	Supply Current (mA)	Product Highlights
HPL-16LC8	Replaces 16L8, 16P8, 10L8, 10H8	5 mA/MHz	• CMOS/TTL Compatible
HPL-16RC4	Replaces 16R4, 16RP4	5 mA/MHz	• Programmable Output Polarity
HPL-16RC6	Replaces 16R6, 16RP6	5 mA/MHz	• 5 mA Output Drive (IOH, IOL)
HPL-16RC8	Replaces 16R8, 16RP8	5 mA/MHz	
HPL-82C339*	Programmable Chip Select Decoder	1 mA/MHz	• $t_{PD} = 25 \text{ ns typ}$

*Available Q1 CY86

For full details, contact: Harris/MHS Semiconductor Sales Ltd., Eskdale Road, Winnersh, Wokingham, Berks, RG11 5TR, England.

Harris Semiconductor: Analog - Bipolar Digital
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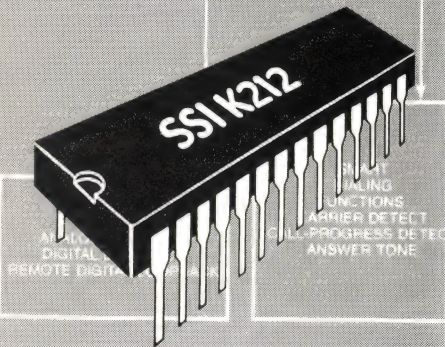


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CIRCLE NO 49

NOW AVAILABLE— THE ONE-CHIP BELL 212A 1200 BPS MODEM



FEATURES:

- One-chip Bell 103/212A compatible modem IC
- Call progress detection and DTMF tone generator on-chip
- Easy to use 8-bit parallel bus (28 Pin DIP, QUAD) or optional serial bus for modem control (22 Pin DIP)
- Interfaces directly with 8051 or 8048 family of microprocessors
- Integrated analog and digital design provides exceptional performance
- Low power CMOS uses a single +10V supply

The SSI K212 is a complete Bell 212A modem on a single chip, and it incorporates all the primary functions needed for a typical intelligent modem. Included on a single chip are full Bell 103 and 212A operating modes, a call progress monitor, and a DTMF dialer. The device also has an 8-bit parallel bus for control of modem functions and will directly interface with the 8048/8051 family of low-cost micro controllers. A complete modem requires only the addition of the phone line interface and a control microprocessor.

The one-chip K212 provides functions on a single chip which were previously only possible using many separate components. The new one-chip modem IC simplifies the design problem for users who are building modems for personal computer applications, and it is ideal for use in any self contained or integral modem system. The K212 provides exceptional performance under poor line conditions, and allows all Bell 212A operating modes.

For more information, contact: **Silicon Systems**, 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, Ext. 595.



CIRCLE NO 83

PRODUCT UPDATE

Dual 12-bit D/A converter has word-wide input path

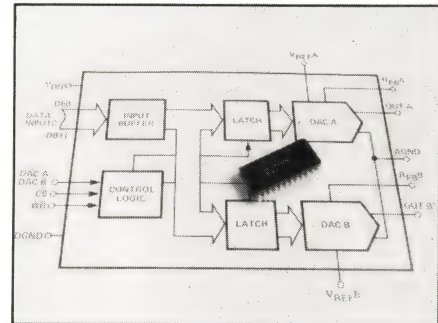
Containing two matched CMOS multiplying D/A converters on one chip, Model DAC-8212 offers 12-bit monotonicity and $\pm 1/2$ -LSB integral linearity over each of its three available temperature ranges: 0 to 70°C, -25 to +85°C, and -55 to +125°C. The device, which is housed in a 24-pin hermetic or plastic double DIP, has a 12-bit input buffer and two 12-bit latches that drive the internal D/A converters.

The word-wide input path makes the DAC-8212 unique in the industry, claims the manufacturer. The converter's closest rival, the dual 12-bit AD7549 D/A converter, uses a 4-bit data-input path. The DAC-8212 requires two processor instructions to update both D/A converters; the AD7549 requires six.

You use the D/A-converter-selection control line, DAC A/DAC B, to direct digital input data to one of the two D/A-converter data latches. The data-load cycle, activated by the \overline{WR} and \overline{CS} control inputs, is similar to the write cycle of a RAM. When you apply logical zero to these control inputs, the data latches are transparent, and digital input data flows directly to the D/A converter selected by DAC A/DAC B.

Offering 4-quadrant multiplication, the converter operates from a single supply that can range from 5 to 15V. The DAC-8212 is available in two accuracy grades, whose respective maximum full-scale gain errors are ± 1 and ± 6 LSB at 25°C and ± 2 and ± 7 LSB over temperature. The multiplying D/A converters require reference-input voltages (V_{REFA} and V_{REFB}). The internal, thin-film R/2R ladder networks present 8- to 15-k Ω impedance to these reference inputs, and the A-to-B impedance match is within 0.1% typ, 1% max.

Worst-case supply current con-



This double-buffered, dual 12-bit D/A converter, the DAC-8212, offers 4-quadrant multiplication. The device contains thin-film R/2R ladder networks and all necessary logic to effect a TTL-level interface with a microprocessor.

sumed by the DAC-8212 is 2 mA, and worst-case power-supply rejection is 0.02%/°C at 25°C and 0.04%/°C over temperature. Output-current settling time to within $\pm 1/2$ LSB of full-scale value is 2 μ sec. Input-to-output propagation delay, measured from the 50%-excursion point of the digital input data to 90% of the final analog-output value, is 220 nsec max.

Maximum output capacitance is 90 pF when all D/A latches are loaded with zeros and 120 pF when all latches are loaded with ones. Digital inputs are TTL compatible, and maximum digital-input currents are $\pm 1 \mu$ A at 25°C and $\pm 10 \mu$ A over temperature. Worst-case capacitance for the digital inputs is 15 pF. Prices range from \$15.26 to \$72.20 (100).—**Bill Travis**

Precision Monolithics Inc., Box 58020, Santa Clara, CA 95052. Phone (408) 727-9222. TWX 910-338-0218.

Circle No 730

SILICON SYSTEMS OFFERS THE ONE-CHIP MODEM THAT'S READY FOR DELIVERY NOW!



More Functions Integrated on a Single Chip

The race to deliver a true single chip 212A modem was won in November, 1985 when Silicon Systems released samples of its K212. The new SSI K212 is a full-featured, 1200 BPS modem in a single 28-pin DIP. It incorporates all the primary functions needed to construct a modem which exceeds Bell 212A performance requirements.

Included on the single chip are complete Bell 103 and 212A operating modes, a call progress monitor, and a DTMF dialer. The device also has an 8-bit parallel bus for the control of modem functions and will directly

interface with the 8048/8051 family of low-cost micro-controllers. Its high functionality, low-power CMOS operation, and efficient packaging facilitate design usage and increase system reliability.

Simplifies Modem Design and Manufacturing

The one-chip K212 represents a new level of integration for modem IC's. It provides functions on a single chip which were previously only possible using many separate components. This new single-chip modem simplifies designs for users who are building intelligent modems, or who wish to incorporate datacommunications capability

into specialized systems. A complete modem requires only the addition of the phone line interface and a control microprocessor. The K212 is ideal for use with any self-contained or integral modem system that incorporates a dedicated microprocessor for control and command interpretation.

Pricing and Availability

The Silicon System K212 one-chip modem is available from stock now. For prices or more product information, contact us today.

Silicon Systems, Telecom Products Division,
14351 Myford Road, Tustin, CA 92680
(714) 737-7110, Ext. 595



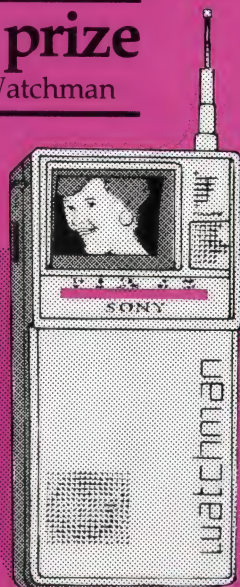
1st prize

Radio Shack Model 14 VCR



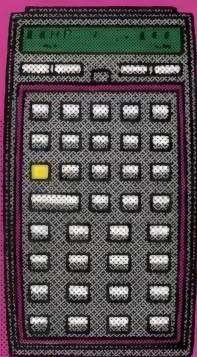
2nd prize

Sony Watchman



3rd prize

H-P 41CV Calculator

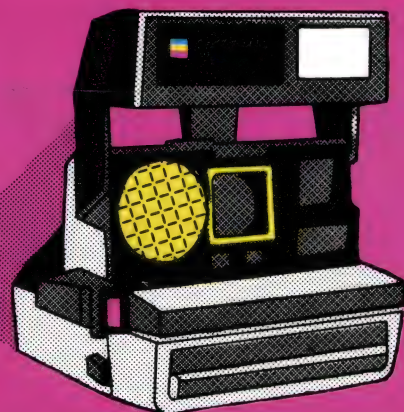


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2. List your selections on the entry card provided.
3. Mail by February 20, 1986.

CONTEST RULES

1. List your top selections on the entry card provided. Be sure to indicate the name of the advertiser (company or organization) and the Information Retrieval Service or Reader Vote number for each advertisement selected. Do NOT use page number. (Ads placed by Cahners Publishing Company, EDN or other Cahners' publications cannot be considered in this contest.)
2. No more than one entry may be submitted by any one individual. Entry blank must be filled in completely, or it will not be considered.
3. To qualify, you must be engaged in electronic design engineering, supervising or managing design engineering, or setting standards for design components and materials.
4. Contest void where prohibited or taxed by law. Liability for any taxes on prizes is the sole responsibility of the winners.
5. Entries that most closely match the rank will be declared winners.
6. Entry cards must be postmarked before February 20, 1986.
7. In case of a tie, the earlier postmark will determine the winner. Decisions of the contest judges will be final.
8. In the event that a prize is not available, publisher may substitute an alternative prize of equal value without prior notice.

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from Radio Shack



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\$50 Gift Certificate
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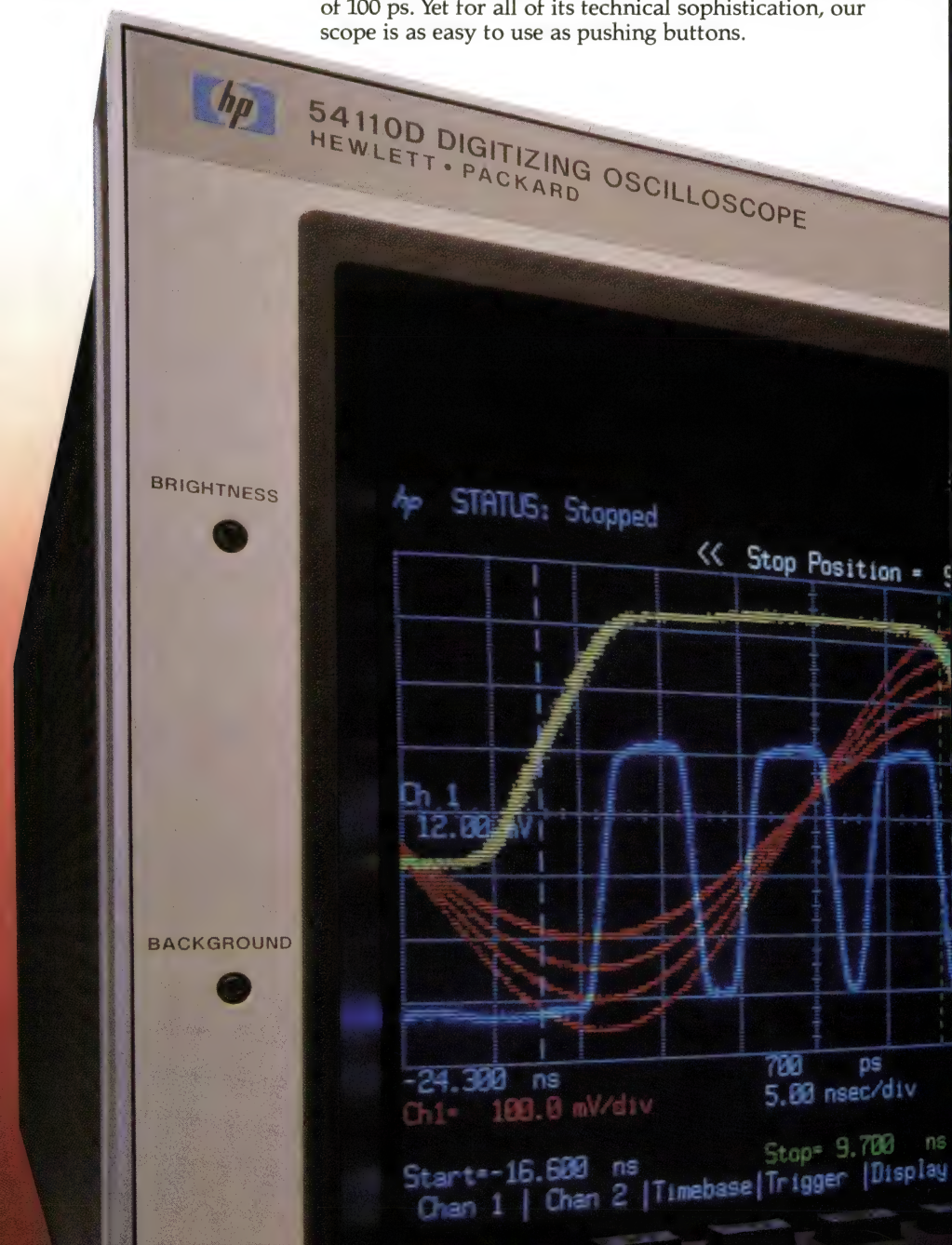
easier. Associate data with traces more efficiently. Customize colors to the application at hand. And emphasize any event or message you choose. So you can use all of our scope's features to best advantage, bringing new shades of productivity to your R&D lab or production test floor.

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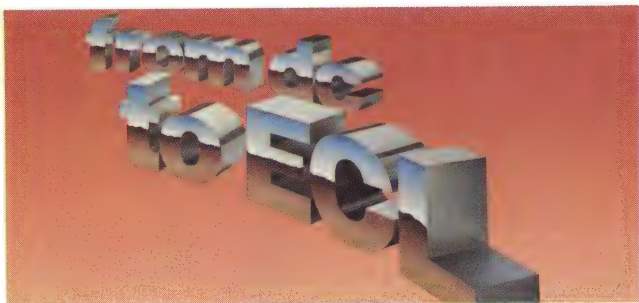


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For more facts on HP's 54110D, call between 8:30 a.m. and 5 p.m. MST. Or contact your local HP sales office listed in the telephone directory white pages. Ask for the electronic instruments department.

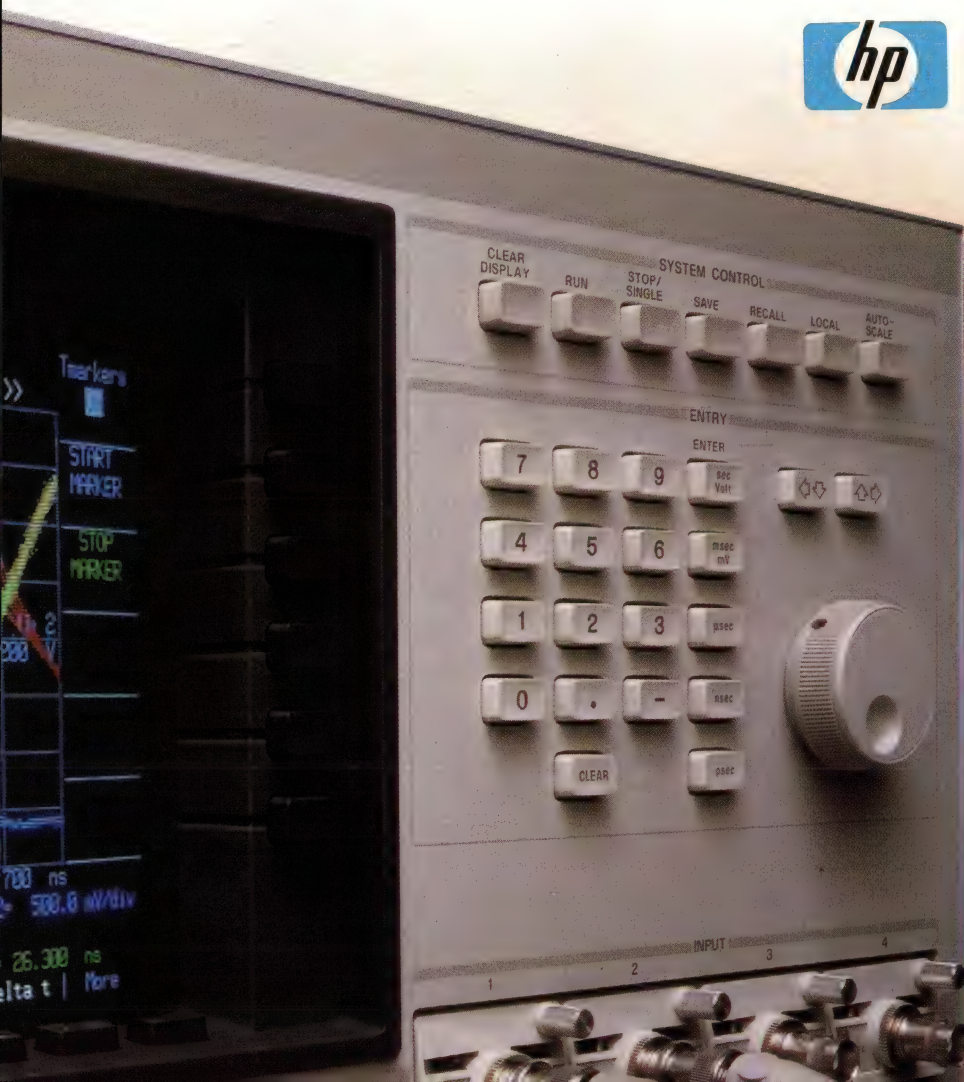
*In Colorado, call collect 590-3490.



**HEWLETT
PACKARD**

CIRCLE NO 15

DS15517



LEADTIME INDEX

Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Last month's average (weeks)	Average (weeks)
TRANSFORMERS								
Toroidal	0	0	82	18	0	0	9.5	9.7
Pot-Core	0	27	64	9	0	0	7.1	8.5
Laminate (power)	0	31	61	8	0	0	6.8	8.8
CONNECTORS								
Military panel	0	25	50	25	0	0	8.5	10.6
Flat/Cable	5	60	30	5	0	0	4.4	5.4
Multipin circular	6	44	28	22	0	0	6.7	8.8
PC	17	39	33	11	0	0	5.2	4.3
RF/Coaxial	0	50	42	8	0	0	5.7	7.1
Socket	30	44	22	4	0	0	3.3	4.2
Terminal blocks	10	60	25	5	0	0	4.0	4.3
Edge card	0	69	26	5	0	0	4.3	6.2
Subminiature	6	59	35	0	0	0	4.0	6.7
Rack & panel	0	33	67	0	0	0	6.0	6.0
Power	0	55	45	0	0	0	4.7	6.6
PRINTED CIRCUIT BOARDS								
Single-sided	0	50	50	0	0	0	5.0	3.7
Double-sided	0	52	41	7	0	0	5.0	5.3
Multilayer	0	31	53	16	0	0	7.4	7.2
Prototype	8	88	4	0	0	0	2.1	2.7
RESISTORS								
Carbon film	41	41	14	4	0	0	2.5	2.7
Carbon composition	27	50	9	14	0	0	3.9	3.8
Metal film	29	46	21	4	0	0	3.3	3.9
Metal oxide	14	43	43	0	0	0	4.3	3.2
Wirewound	13	48	35	4	0	0	4.4	8.1
Potentiometers	17	37	33	13	0	0	5.4	5.4
Networks	27	27	46	0	0	0	4.2	5.1
FUSES								
	35	40	25	0	0	0	2.8	2.6
SWITCHES								
Pushbutton	19	48	28	5	0	0	4.0	3.5
Rotary	11	31	42	11	5	0	7.1	4.2
Rocker	0	43	50	7	0	0	6.0	5.3
Thumbwheel	8	33	42	17	0	0	6.7	7.1
Snap-action	17	58	25	0	0	0	3.2	4.9
Momentary	0	67	25	8	0	0	4.7	6.1
Dual-in-line	6	69	25	0	0	0	3.4	5.2
WIRE AND CABLE								
Coaxial	35	47	18	0	0	0	2.4	2.5
Flat ribbon	37	47	16	0	0	0	2.2	3.1
Multiconductor	18	59	23	0	0	0	3.1	4.1
Hookup	37	58	5	0	0	0	1.6	1.3
Wirewrap	54	38	8	0	0	0	1.4	1.7
Power cords	26	52	17	5	0	0	3.1	3.8
Other	50	17	33	0	0	0	3.0	6.6
POWER SUPPLIES								
Switching	5	42	37	16	0	0	6.3	8.4
Linear	0	50	37	13	0	0	6.0	6.1
CIRCUIT BREAKERS								
	20	20	53	7	0	0	5.7	5.8
HEAT SINKS								
	24	38	33	5	0	0	4.2	3.9

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Last month's average (weeks)	Average (weeks)
RELAYS								
General purpose	30	10	50	10	0	0	5.8	4.8
PC board	12	23	53	6	6	0	7.2	6.3
Dry reed	0	50	50	0	0	0	5.0	4.6
Mercury	0	14	86	0	0	0	7.1	6.3
Solid state	15	15	62	8	0	0	6.5	6.4
DISCRETE SEMICONDUCTORS								
Diode	32	35	30	0	0	3	4.0	5.0
Zener	30	33	33	4	0	0	3.9	4.0
Thyristor	13	40	40	7	0	0	5.1	4.2
Small signal transistor	33	24	38	5	0	0	4.3	3.2
FET, MOS	7	47	33	13	0	0	5.7	5.6
Power, bipolar	20	27	53	0	0	0	4.8	5.9
INTEGRATED CIRCUITS, DIGITAL								
CMOS	18	36	32	14	0	0	5.6	5.1
TTL	34	23	35	4	4	0	4.8	5.8
LS	25	43	25	4	3	0	4.4	6.0
INTEGRATED CIRCUITS, LINEAR								
Communication/Circuit	15	31	39	15	0	0	6.2	6.0
OP amplifier	10	48	28	14	0	0	5.5	5.8
Voltage regulator	14	52	29	5	0	0	4.1	5.0
MEMORY CIRCUITS								
RAM 16k	8	38	46	8	0	0	5.7	5.1
RAM 64k	41	29	30	0	0	0	2.9	4.4
RAM 256k	19	44	31	6	0	0	4.4	5.7
ROM/PROM	14	57	29	0	0	0	3.4	7.2
EPROM	23	38	29	10	0	0	4.6	6.0
EEPROM	15	38	39	8	0	0	5.1	5.7
DISPLAYS								
Panel meters	17	17	58	0	8	0	7.2	5.0
Fluorescent	0	33	67	0	0	0	6.0	6.1
Incandescent	14	14	72	0	0	0	6.0	5.3
LED	11	50	33	6	0	0	4.6	5.3
Liquid crystal	0	12	63	25	0	0	9.3	8.2
MICROPROCESSOR ICs								
8-bit	31	38	31	0	0	0	3.3	6.9
16-bit	19	37	44	0	0	0	4.3	7.9
FUNCTION PACKAGES								
Amplifier	0	44	56	0	0	0	5.3	6.8
Converter, analog to digital	0	40	50	10	0	0	6.4	6.7
Converter, digital to analog	0	25	58	17	0	0	7.8	7.2
LINE FILTERS								
	0	33	67	0	0	0	6.0	5.4
CAPACITORS								
Ceramic	32	43	21	4	0	0	3.1	5.2
Ceramic monolithic	18	36	36	10	0	0	5.1	4.2
Ceramic disc	40	32	20	4	4	0	3.9	3.5
Film	17	48	26	9	0	0	4.4	4.8
Electrolytic	24	52	16	8	0	0	3.6	5.5
Tantalum	18	41	26	15	0	0	5.3	5.3
INDUCTORS								
	25	33	42	0	0	0	4.0	4.0

Source: Purchasing magazine's electronic business survey

Megahurts

The pain starts when you need your sales rep. And he doesn't seem to need you.

It gets worse when you place your order. And they place you on a waiting list.

It peaks when you need service. And they take more money than you expected. And more time than you've got.

Megahurts. When dealing with your test and measurement company gives you a giant pain.

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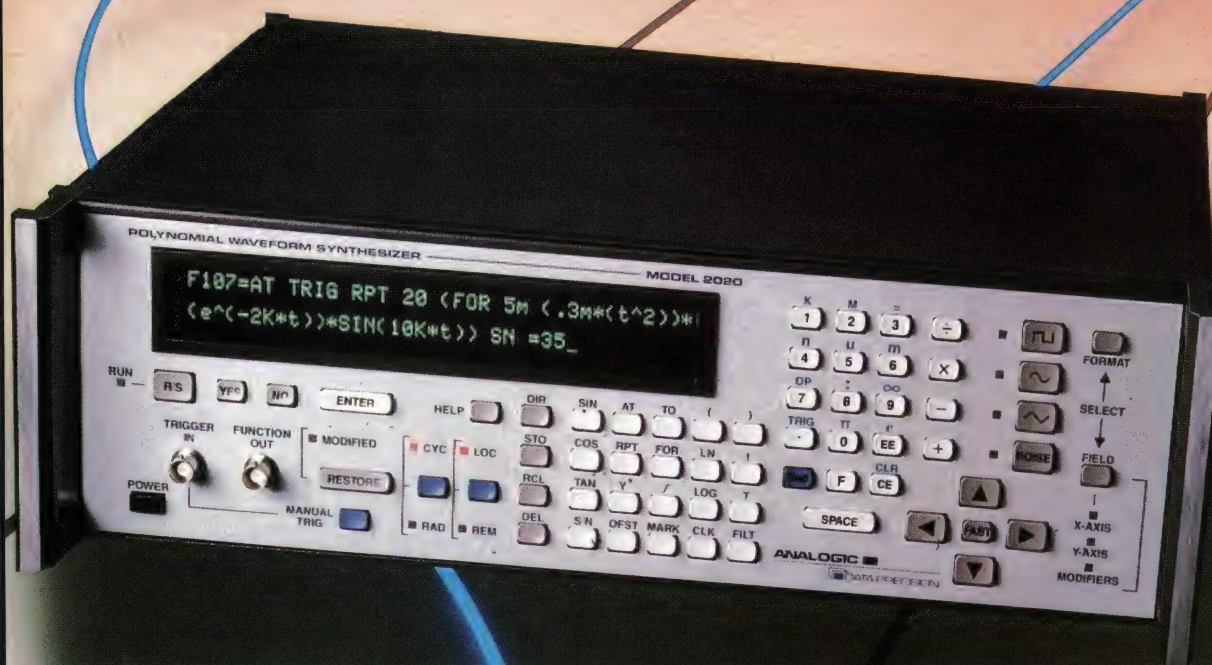
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PHILIPS
Test the difference.

The image shows the Analogic Model 2020 Polynomial Waveform Synthesizer, a black rack-mounted device. The front panel features a digital display showing the equation: $F107=AT \text{ TRIG RPT } 20 \text{ (FOR } 5M \text{ (.3M*(t^2)))*I (e^{(-2K*t))}*SIN(10K*t)) \text{ SN } =35_$. Below the display is a control panel with various buttons and knobs. The buttons include a numeric keypad (0-9), function keys (DIR, SIN, AT, TO, STO, COS, RPT, FOR, LN, RCL, TAN, LOG, Y, DEL, SN, OFST, MARK, CLK, FILT), and a set of modifier keys (K, M, =, +, -, *, /, ^, %, ~, ~~, ~~~, ~~~~). There are also buttons for RUN, RS, YPE, NO, ENTER, HELP, MODIFIED, RESTORE, CYC, LOC, RAD, REM, TRIGGER IN, FUNCTION OUT, MANUAL TRIG, POWER, and a set of directional arrows. The device is set against a background of a red and blue abstract graphic with geometric lines.





Math Formula Entry Lets You Set The Rules

The DATA 2020 is a revolutionary new waveform generator with the ability to synthesize waveforms directly from mathematical formulas. Instead of using manually entered approximations, the DATA 2020 calculates hundreds, even thousands, of points to smoothly define a waveform. Simply key in the expression representing the desired waveshape and its duration on the instrument's front panel in the form $Y=f(t)$. The DATA 2020 provides function keys such as *sine*, *cosine*, *tangent*, *log*, *ln*, y^x , and *integral* to speed equation entry. For example, the waveform at the top of this page was generated from the formula:

$$Ae^{-bt} \sin \omega t.$$

Using the waveform synthesis technique, the DATA 2020 can generate waveforms which are very close realizations of their mathematical ideals, enabling the DATA 2020 to set the standard for waveform fidelity.

High Performance Features

High resolution, high speed and a high degree of mathematical accuracy enable the 2020 to deliver on its promise. Every waveform generated through Math Formula Entry benefits from the full 12-bit D/A range independently of output amplitude. A data point duration as brief as 40 ns (25 MHz output clock rate) allows more points to define the waveform.

The 2020 also features high stabilization timing plus 24-bit IEEE floating point arithmetic for optimum accuracy.

Deep Waveform Memory

The DATA 2020 provides an exceptionally large output memory—up to 128K points—and then expands this impressive capability even further with the memory management techniques of *constant compression* and *dynamic looping*.

Through its unique waveform storage approach, the DATA 2020 can store the necessary information to generate hundreds of unique waveforms in its large, non-volatile waveform equation library.

Arbitrary Waveform Generation

The DATA 2020 can also create waveforms through virtually every other accepted generation method including Point Entry, Line Segment, Scope Draw, and Down Loading from remote sources via IEEE-488 and RS-232 interfaces. The 2020 also accepts and regenerates waveforms acquired by Data Precision's DATA 6000 Universal Waveform Analyzer. What was transient can become repetitive!

When you need simply a sine, square or triangle wave, the DATA 2020 has standard functions available at the touch of a button. The DATA 2020 also includes white noise generation as a standard function, and provides the ability to sum white noise with any waveform.

Power For Your Application

The DATA 2020 replaces a roomful of signal sources, filters, combiners and specialized tuned circuits to bring you total waveform control in one compact, powerful and easy to use instrument. Consider the DATA 2020 for your applications in production ATE, vibration stimulus, acoustic modeling, radar, video and digital simulation—any environment that frequently needs unique or complex waveforms.

The DATA 2020 Polynomial Waveform Synthesizer: the first . . . and only instrument that gives you the power to rule the waves.

With the New DATA 2020 Polynomial Waveform Synthesizer.

See Us at ATE WEST booth numbers 1524 and 1526

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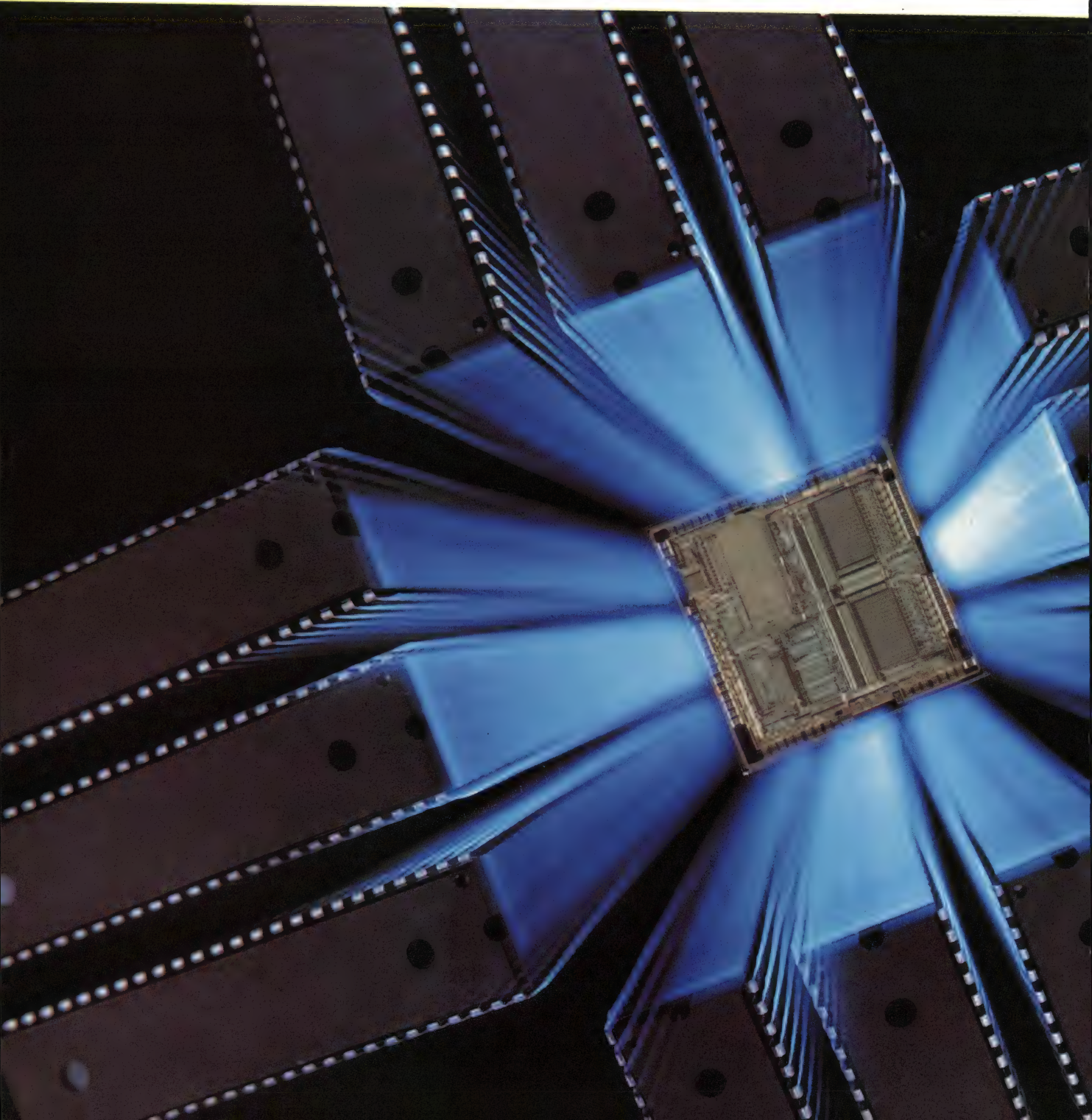
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Special Report

Enhanced 1-chip



μ Cs

Choosing among today's enhanced 1-chip μ Cs, which offer an ever-expanding array of options, can be more difficult than choosing a large computer. The chips range from 4-bit devices with limited ROM to sophisticated 16-bit μ Cs with many features. Performance and cost remain the dominant selection criteria for most designers.

Jon Titus, *Senior Editor*

Among the many features and attributes that today's enhanced 1-chip μ Cs offer, price and performance are the two most important factors in designers' product choices. To properly evaluate a chip's performance and cost, however, you should consider both the engineering and the strategic aspects of the device. On the engineering side, consider such factors as the amount of on-chip ROM and RAM, the number of I/O lines, and a device's off-chip expansion capabilities. On the strategic side, think about second sources, expansion within a family, and the breadth of a company's product offerings. You'll find that choosing a 1-chip enhanced μ C from today's variety of chips and manufacturers can be more difficult than choosing a large computer.

Four- and 8-bit μ Cs still dominate

Although new μ Cs feature 16-bit architectures, 4- and 8-bit chips have the microcontroller field almost to themselves. Rather than offer new architectures, most manufacturers add features to existing designs. In the μ C realm, a processor's bit width is less important than its performance.

One-chip μ Cs range from 4-bit devices with limited I/O capabilities and a small amount of ROM to sophisticated devices with a multitude of features. Newer chips provide such enhanced features as special-purpose I/O lines, serial communication ports, EEPROMs, and analog-to-digital converters. Unfortunately, the variety of features increases the difficulty in making a choice for your application. To help narrow your choice, start by examining what the chips have in common.

On-chip read-only and read-write memory is common to all μ C families. The read-only category includes mask ROM, EPROM, and EEPROM. All μ C manufacturers offer mask programming, and mask

Offering a variety of options, today's enhanced 1-chip μ Cs range from simple 4-bit devices to sophisticated 16-bit units with many features. (Photo courtesy Intel)

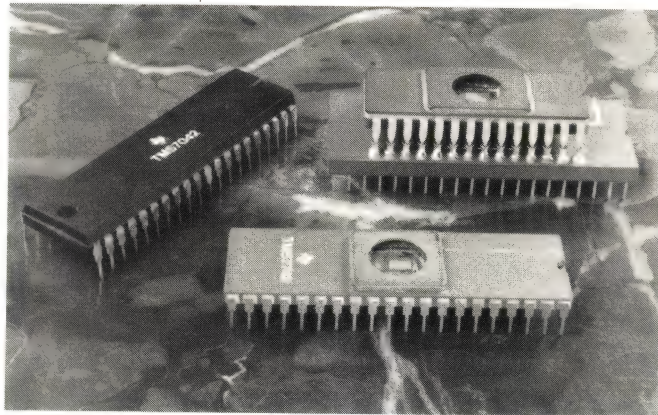
Four- and 8-bit CPUs still dominate the μ C market.

charges usually range from \$2500 to \$3500. Delivery times for mask-ROM samples are generally four to 16 weeks; during 1985, however, leadtimes for 8051-type chips stretched to 20 weeks.

If in a year you'll use fewer than 5000 chips with one mask-ROM pattern, consider the other program-storage devices—EPROMs, one-time-programmable (OTP) ROMs, and EEPROMs. Devices with an on-chip EPROM also contain a quartz window that lets you erase the EPROM's contents with an ultraviolet light. After erasing the data and program steps, you can reprogram the chip with new information. Devices with internal or piggybacked EPROM are useful during product development when you need only a few chips for testing and debugging. Along with the EPROM-based μ C chips, you'll need a PROM programmer that meets the requirements of the chips.

Some μ Cs accept standard EPROMs in piggyback sockets. You can leave the μ C chip in your prototype and program the standard EPROMs without buying special PROM-programmer personality cards that support specific EPROM-based μ Cs. Unfortunately, internal- and piggyback-EPROM μ Cs are expensive: The 8751 μ C chips sell for \$30 to \$35 (25,000), and the 8-MHz Z8 piggyback EPROM chip (Z8603) costs \$14.95 (1000). Keep in mind that most manufacturers specify ROM and EPROM in bytes. For example, even though the Toshiba TLCS-42 and -47 μ C families are 4-bit devices, memory capacities are listed in 8-bit bytes.

As an alternative to EPROM-based program storage, consider chips that contain electrically erasable PROM (EEPROM). Working in collaboration with Texas Instruments, Seeq Technology includes 1k byte of EEPROM in the 72710 μ C—a relative of Texas Instruments' TMS7000 μ C family. Samples of the chip are available, and the company expects to offer a 72720 chip with 2k bytes of EEPROM in early 1986. Motorola's latest offering, the MC68HC805C4, lets you use 4k bytes of EEPROM in two independent blocks. You can write into one block while reading from the other. Motorola expects to ship samples of the MC68HC805C4 in early 1986. The MC68HC11, which costs \$68.11, includes 512 bytes of EEPROM as well as 4k bytes of customizable mask ROM and 256 bytes of RAM. The 68HC11 includes the EEPROM in its main memory map so you can store program steps in it. However, the chip provides 4k bytes of ROM, so the most efficient use of the EEPROM is for storing information. You could also use the EEPROM to hold data or special program steps that customize a μ C.



Piggyback EPROM chips and internal EPROMs, like these from Texas Instruments, simplify software development. You develop hardware concurrently because the EPROMs don't force you to give up I/O lines as you would for external memory expansion.

General Instrument's PIC1600 line includes two chips that contain both ROM and EEPROM. Unlike the 68HC11, you can't run programs from the 32 EEPROM-storage registers. Along with EEPROM, the PIC16E53 contains a 256 \times 12-bit program ROM; the PIC16E57 furnishes a 512 \times 12-bit mask customizable ROM. The manufacturer claims a 10-year data-retention period for the EEPROM registers over -40 to +85°C. Each chip sells for less than \$3 (50,000).

μ Cs require no PROM programmer

An advantage of EEPROM-based μ C chips is that you program them in situ, so you don't require a PROM programmer or an erasing lamp. Likewise, the EEPROMs require no special programming voltages. EEPROMs offer many erase-write cycles, leading to reliable data storage. In addition to storing programs, you can use EEPROMs to store and update phone numbers for modems, statistical data for product analysis, and diagnostic information for field servicing.

Taking an alternate route to including EEPROM within a μ C, NCR provides EEPROMs within its macroelectronic cell library for the 65CX02 core μ P. Incorporating the EEPROM in a μ C design adds only one step to the traditional CMOS-fabrication process. Containing 2k bytes of EEPROM, the 65C00/1E μ C also includes RAM, bidirectional I/O lines, and a counter/timer circuit.

Read-write memory, or RAM, which provides temporary storage, is an important part of μ C chips. The chips treat RAM in two ways: either as temporary storage registers apart from the main memory space or as read-write memory within the main memory space.

Such processors as Zilog's Z8 and Super Z8 treat the internal RAM as a set of storage registers. The Z8 provides 128 registers while the Super Z8 furnishes 272. Likewise, the RAM in Toshiba's TLCS-47 and -42 μ Cs is available as internal data-storage registers.

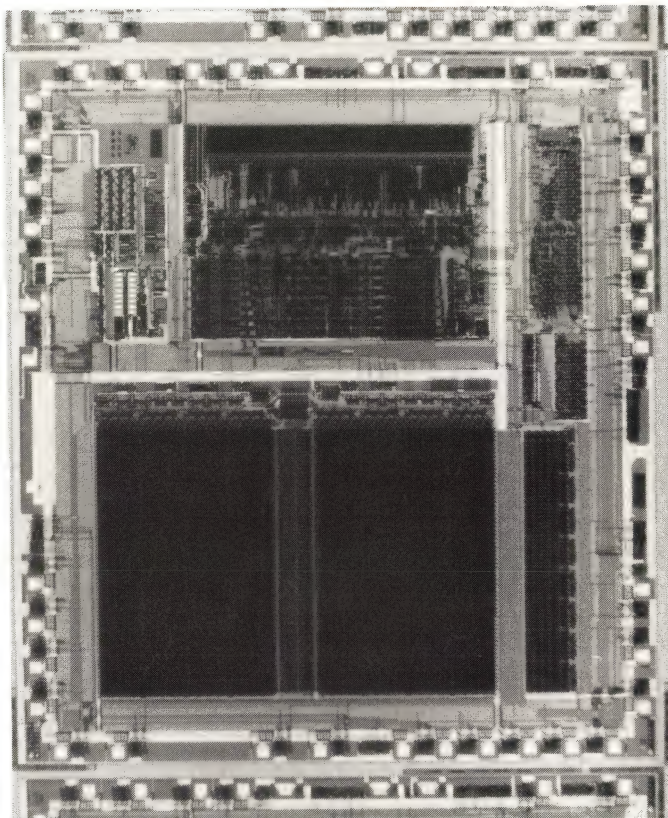
On the other hand, the Intel 8096 contains 256 bytes of RAM over addresses 00_{16} through FF_{16} in the chip's 64k-byte address space. Of the 256 internal locations, 230 are available for general-purpose use. Although you address the RAM within the 8096's memory-address space, you can't execute the program steps stored there. An attempt to execute code in the RAM forces the chip to address external memory, an area that Intel reserves for its development systems.

Other μ C chips also map their internal RAM into their memory-address space. Motorola's 6800 μ C family maps internal RAM into the total address space available to the CPU. The Rockwell R65C00/21 μ C contains 128 bytes of RAM between addresses 80_{16} and FF_{16} in address-page zero, a critical page in 6502-type μ P and μ C systems. The 65C00/21 is unique among μ C chips because it contains two independent CPU sections that share the I/O ports and internal memory. Each CPU has its own set of registers.

Although RAM in main memory (program memory) and RAM in registers (data memory) may appear similar, the subtle differences between them affect software development. General-purpose assemblers don't distinguish between memory types; instead, they assume that addresses run continuously within one block. As a result, you'll have to choose your register definitions carefully and declare them separately from memory assignments. Software development can be complex, so you'll have to keep in mind the limited memory resources on your μ C.

For example, excessive use of subroutines and stack-storage spaces—often effective in larger computers—can have disastrous effects in μ Cs. The Toshiba TLCS-42 lets your software use only one subroutine at a time. Subroutine nesting is impossible. General Instrument's PIC16E57 provides a 2-level subroutine stack, and the Toshiba TLCS-47 provides for 15 levels of subroutines, probably enough for most tasks. However, if your control application requires several external interrupts, the stack can grow quickly. Even if you don't use external interrupts, keep in mind that internal clocks, timers, counters, and I/O ports generate interrupts.

In most applications, the stack uses internal RAM locations for temporary storage. As the stack area grows, it reduces the storage space available. In the



The 65C00/1E μ C chip from NCR contains internal EEPROM. Depending on your system's needs, you can select EEPROM from NCR's standard library of functions. The library also includes analog cells.

Zilog Z8 family, the Z8601 chip contains 124 RAM locations for register and stack use. Each interrupt requires three stack locations and each subroutine call requires two. Allocate RAM carefully to prevent the stack from crashing into your data.

Off-chip memory provides flexibility

For applications that require ROM or RAM beyond that available in a μ C chip, consider expanding memory outside the chip. Most 8-bit μ C families have some form of off-chip expansion capability—you add memory chips to increase RAM or ROM capacity. Some chip families also provide ROMless μ Cs, and you must supply an external ROM or PROM that contains your program. The off-chip expansion technique is well suited to short runs of a product or to prototypes headed for beta-site testing. If tests show that you'll need more ROM or RAM, you plug in the extra chips and retest the product without committing to a new mask ROM. Should you need more or less memory in the final

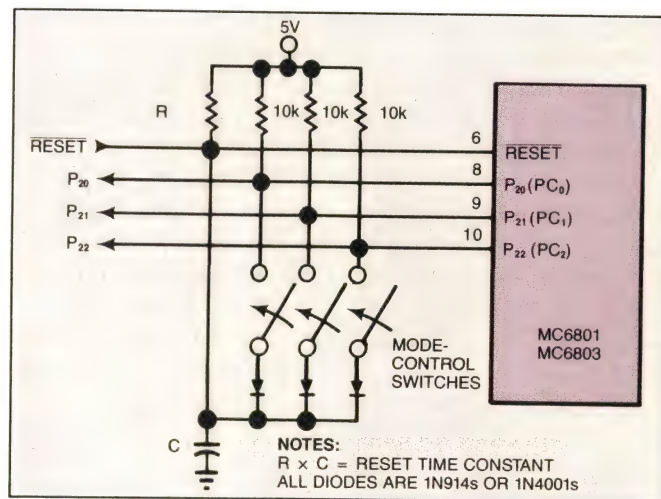
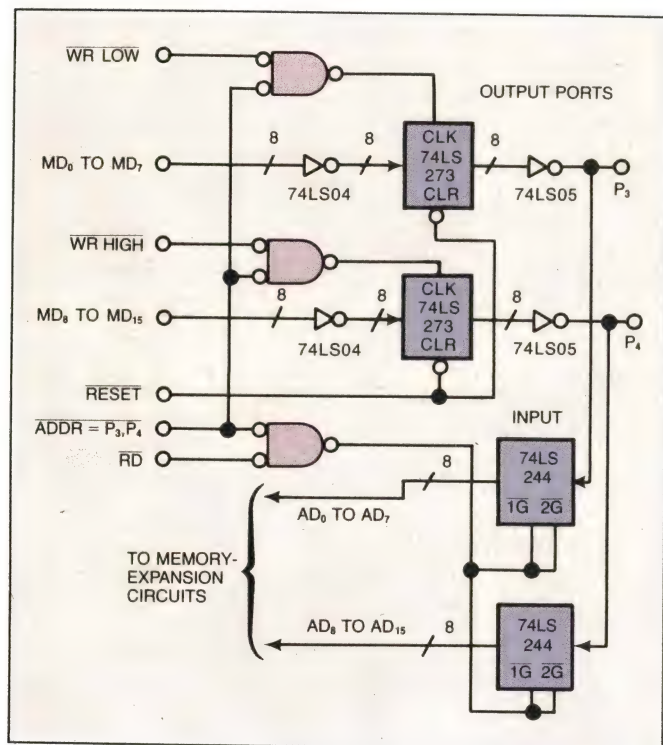


Fig 2—External switches set a 6801/6803 into expansion modes. Add the switches only if you'll need to expand the μ C beyond its 1-chip mode.

Fig 1—Added circuits provide I/O ports for the Intel 8096 when you expand the chip's memory. The external I/O ports let you maintain all of the I/O lines while you develop software in an external RAM or PROM.

product, choose the μ C that best suits your requirements.

If you sell small quantities of products that require different programs, consider using an off-chip EPROM to store the programs and data. You'll need only one type of EPROM chip and one type of μ C chip in inventory. Doing your own EPROM programming lets you make changes and modifications without paying an additional mask charge. Unfortunately, off-chip EPROMs have a disadvantage: Your competitors can pull out the EPROM and examine your program. For software security, a device such as Intel's 27916 keyed-access EPROM (KEPROM) provides a lock against unauthorized access.

Also consider whether someone can read the contents of your ROM, even if it's part of the μ C chip. Some chips provide ROM outputs. Seeq's 72710 chip features a mechanism that locks the CPU in the single-chip mode. Although the single-chip mode gives the CPU access to the EEPROM, you can't read its contents. To remove the EEPROM lock, you must first erase the EEPROM's contents.

Expansion requires I/O lines

Despite the security risks, off-chip ROM and RAM have several advantages. First, the external memory space is larger than the μ C's internal memory space.

The larger memory size lets you concentrate on accomplishing tasks without first trying to optimize the program for a 2k-byte internal ROM. Optimization comes later—after you test the software. Also, systems with low-cost EPROMs, RAMs, and ROMless μ Cs often are less expensive than μ Cs with on-chip EPROM. However, the use of off-chip memory exacts a penalty in the number of I/O lines available.

Manufacturers provide parallel I/O ports that function in several ways. You can program the ports so they operate as I/O lines, control lines, serial communication lines, or analog inputs. The parallel ports can also serve as expansion data and address buses. The Texas Instruments TMS7000 family operates in a single-chip, peripheral-expansion, full-expansion, or microprocessor mode. In its single-chip mode, the TMS7742 chip provides 22 bidirectional I/O lines, two input lines, and eight output lines. However, when put in its full-expansion mode, it reserves ports for the address and data signals that connect the CPU to the external memory chips. The full-expansion mode leaves only six I/O lines (two input lines and four output lines) for peripheral-device control.

The Intel 8096 lets you access memory locations within the chip's 64k-byte address range. If the CPU attempts to address memory that is unavailable in the

*For short production runs, consider
EPROM- or EEPROM-based μ C chips.*

chip, 16-bit data and address information appears in multiplexed form at two 8-bit I/O ports. Even if you want to expand only a portion of the chip's memory space, you lose all 16 I/O lines. By adding latches and buffers, you can reconstruct the two I/O ports, thereby retaining their functions (Fig 1). Although the external logic seems to defeat the purpose of a 1-chip μ C, it gives you the option of using external memory for software development while still having the I/O ports available for system development. When you finish your development work and put the program in internal ROM, the two ports revert to normal use for I/O-device control and data transfer. Keep in mind that the 8096 chip's internal port lines and the external port circuit have different electrical and timing characteristics.

Motorola's MC6801 and MC6803 let you expand the address space in stages from completely internal to an external 64k-byte range. Both chips offer eight expansion modes that you set with external connections (Fig 2). In five of the expanded modes, one 8-bit port multiplexes 8-bit bidirectional data and the least-significant address bits, A_7 to A_0 . A second 8-bit port provides the most-significant address bits, A_{15} to A_8 . You use as few or as many of the A_{15} to A_8 address lines as you need. Lines that you don't select for use as address outputs act as standard digital-input lines.

Not all μ C chips offer off-chip EPROM or RAM expansion. Don't fault the manufacturers for leaving out the expansion capabilities, however. Their chips are

meant for low-level, low-cost applications where off-chip expansion isn't economical. For example, you can't expand the internal memory of General Instrument's PIC1600 μ C family, nor can you expand National Semiconductor's 4-bit COPS family of μ Cs.

Chips offer varied I/O functions

When not used for expansion, μ C I/O ports provide a variety of functions that make the chips powerful control devices. Typical I/O ports provide

- Vacuum-fluorescent-display drivers
- Liquid-crystal-display drivers
- LED drivers
- Counter inputs
- Bidirectional logic lines
- A/D-converter inputs
- Interrupt and test inputs
- Phase-lock-loop controls
- PWM outputs
- Timer outputs
- Serial I/O connections.

Among the newest additions to the lineup of I/O functions are specialized serial ports, A/D converters, and I/O drivers for displays. Recently introduced μ C chips provide two types of serial I/O connections: UART signals for general-purpose communications and special serial-protocol signals for chip-to-chip communications. The serial port on SGS Semiconductor's M38730—a member of the 3870 family—represents a typical UART

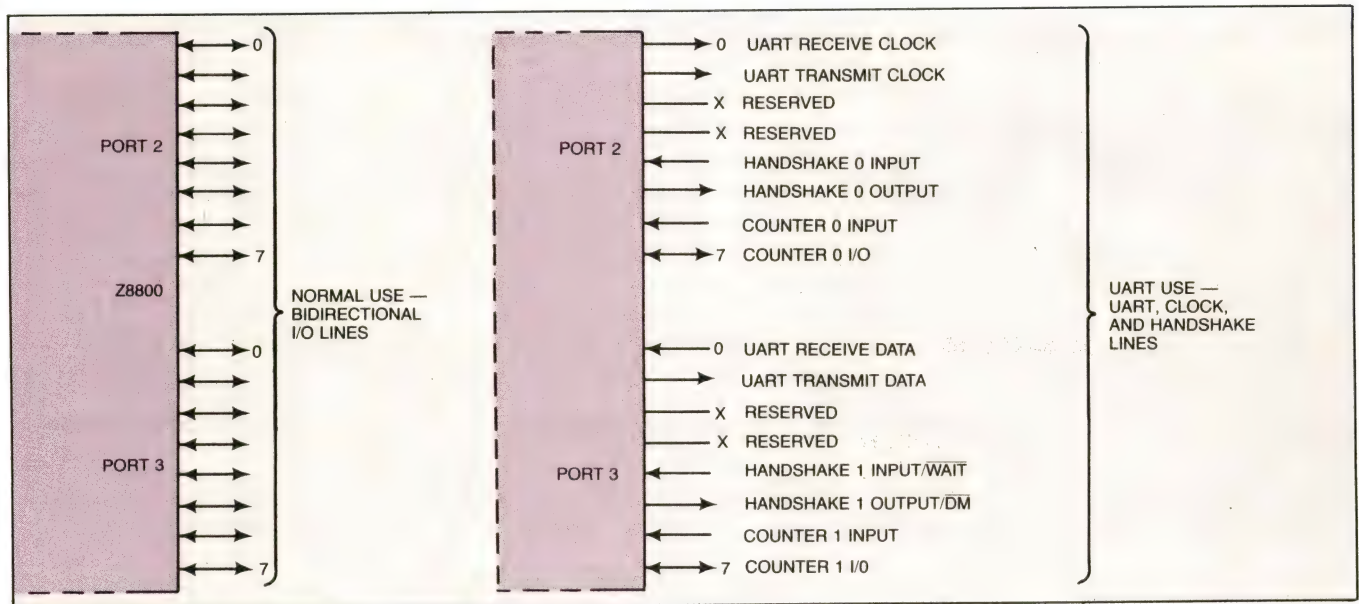


Fig 3—Although several lines provide clock and handshake-signal outputs, the Zilog Super Z8 requires two ports for its UART.

Most 8-bit μ Cs let you expand RAM and ROM outside the chip.

port. You can operate the UART at one of nine internally generated baud rates, and you can select a word length for transmission and reception. The serial controller provides programmable stop-bit and parity options. Although most UART circuits allow a maximum word length of eight data bits, the M38730 allows as many as 16.

UARTs absorb I/O lines

To take advantage of a serial port, you'll usually have to give up several parallel I/O-port lines. For example, in Zilog's ROMless Super Z8, I/O ports 2 and 3 provide the UART signals as well as several control signals (Fig 3). National Semiconductor's 16-bit high-performance controller family (HPC16140) includes UART functions in all μ C chips; however, you sacrifice a 16-bit and an 8-bit I/O port to obtain the UART functions. Not all of the 24 I/O lines relate to UART operations. Many of the non-UART signals provide timer outputs, interrupt inputs, and other control signals. Expect samples of the HPC family in early 1986.

When your application requires an internal UART function, you may lose an internal general-purpose counter/timer as well as I/O ports. Texas Instruments' TMS7742 includes three general-purpose 8-bit timers. When you use the chip's internal UART, however, one timer provides the baud-rate clock signal that controls serial data-transfer operations.

Many μ C manufacturers include special-purpose serial ports on their chips. Unlike the UART function, which supports standard data-transfer operations be-

tween the μ C chips and many types of equipment, the special serial functions are meant for chip-to-chip communications. The serial peripheral-interface (SPI, Motorola), inter-IC (I^2C , Signetics/Philips), and Microwire (National Semiconductor) protocols are the most common (Fig 4). The special serial protocols let μ C chips transfer information between peripherals and other μ C chips over two or three wires.

The price you pay for a simple serial bus is speed—the maximum clock rate for transfers between Motorola's SPI chips is 1.05 MHz. However, consumer products don't require microsecond response times. The popularity of the specialized serial buses depends on how quickly chip manufacturers support them. Motorola plans to provide SPI chips with memory, a real-time clock, and A/D-converter functions, and Signetics/Philips offers a variety of I^2C -bus chips.

Along with special serial-communication channels, you'll find that many μ Cs include an 8- or 10-bit A/D converter (Table 1) that has at least four analog-input channels (Fig 5). Selecting analog-input lines is similar to choosing serial-port and memory-expansion configurations: It's a tradeoff for the available I/O lines. Only the Siemens SAB 80515/80535 provides eight dedicated analog-only input lines. Motorola's MC6805R family requires seven lines of an 8-bit input port, even if you want to measure only one unknown voltage. The 8-line input port supplies four analog-input lines, a digital input, and an interrupt input. You must provide reference voltages on the two remaining lines.

Flexible input arrangements in the 8096, HPC16140,

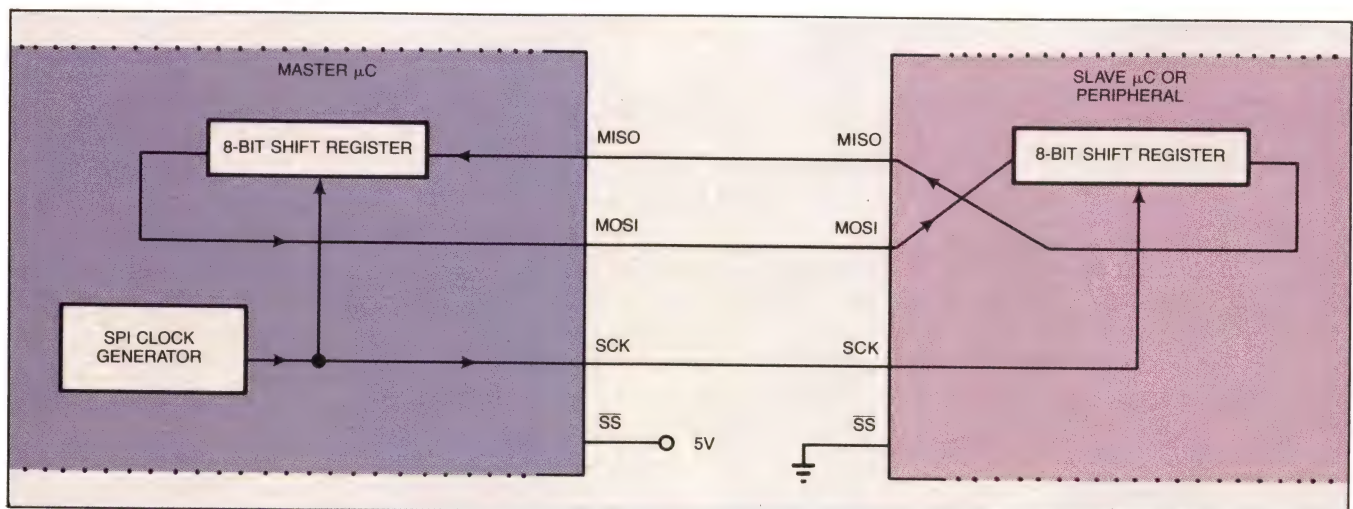


Fig 4—Local serial I/O buses link μ Cs and I/O chips in a simplified scheme that transfers data at low rates, usually less than 2 MHz. Several manufacturers offer special serial I/O and peripheral support chips.

TABLE 1— μ C FAMILIES WITH SPECIAL I/O FEATURES¹

μ C FAMILY	STANDARD UART	SPECIAL SERIAL PORT	INTERRUPT	BIDIRECTIONAL PORTS	INPUT-ONLY PORTS	OUTPUT-ONLY PORTS	TIMER- COUNTER	VFD DRIVERS	LCD DRIVERS	LED DRIVERS	DTMF OR SOUND	A/D CONVERTER	PLL CONTROL	PWM CONTROL
ADVANCED MICRO DEVICES 8751/9761
FUJITSU 4-BIT FAMILY ²
GENERAL INSTRUMENT PIC7000
HITACHI HD63701 HMCS40
INTEL 8096 8051
MITSUBISHI 740
MOTOROLA 6801/6803 6805 6811
NATIONAL SEMICONDUCTOR COPS HPC 16140
NEC 7800 78000 μ COM4 μ PD7500
NCR 6500
RCA 6805
ROCKWELL R6500
SGS SEMICONDUCTOR 3870
SHARP SM
SIEMENS 80515/80535
TEXAS INSTRUMENTS 7000
TOSHIBA TLCS-47	NOTE 3
ZILOG Z8

NOTES:

1. NOT ALL CHIPS WITHIN A FAMILY HAVE ALL THE FEATURES INDICATED.
2. ALSO INCLUDES A D/A CONVERTER.
3. SHIFT-REGISTER OUTPUT/INPUT (4 BITS).

External memory has a disadvantage—it's difficult and expensive to protect your software.

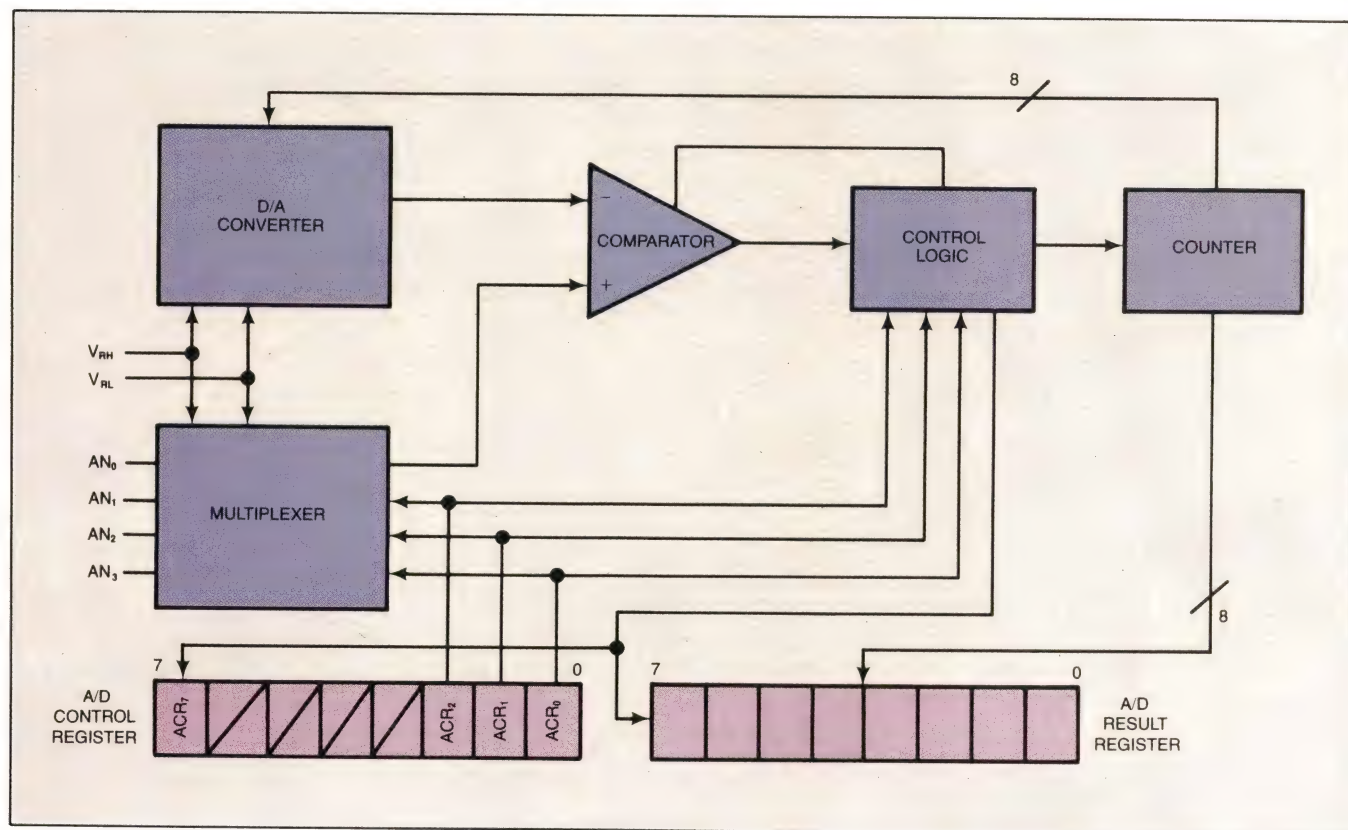


Fig 5—A typical 6805 μ C's internal A/D converter provides an input multiplexer, D/A converter, and control logic. Registers provide multiplexer-selection bits, the conversion result, and a flag signal.

and 38ADP70 μ C chips supply the connections between external devices and internal A/D converters. Each of the three chips contains an 8-line input port capable of selecting individual digital and analog inputs. If you have three analog signals to measure, you'll need only three analog-input lines. You can use the five remaining lines for digital inputs.

Using an on-chip A/D converter requires caution. If the A/D converter includes no S/H amplifier, the unknown voltage applied to the converter must remain stable during the conversion. Long conversion times and the lack of an S/H amplifier render your measurements inaccurate if the unknown signal has high-frequency components. In the 8096, for example, conversions require 42 μ sec. For a 5V full-scale range and $\pm 1/2$ -LSB accuracy, the input voltage can't change more than ± 2.4 mV during the conversion. Using the formula

$$\Delta V/\Delta t = (2\pi F)(\text{Peak Voltage}),$$

you'll find that for a 5V full-scale signal, the maximum frequency can be no greater than 3.8 Hz. To make best

use of the A/D converter on the 8096 chip, you'll need an external S/H amplifier for each analog input. Intel notes that when the 8096 chip connects an input to the A/D converter, that input's impedance drops to a value lower than normal. So, if you don't use an S/H amplifier, the input may still require a buffer amplifier. Rather than use one of the newer μ Cs with an on-chip A/D converter, you may find it less expensive to use a discrete A/D converter and a simpler μ C.

In addition to A/D converters, some μ Cs contain special output ports. Such ports include vacuum-fluorescent-display (VFD) drivers, liquid-crystal-display (LCD) drivers, LED drivers, pulse-width-modulator (PWM) drivers, and tone generators. Although the VFD drivers provide high-voltage output lines that directly drive the VFD tubes, your software must multiplex the display's segment information onto the output lines. Mitsubishi's M50757 μ C chip lets you use as many as 18 outputs as high-voltage display-driver lines. You'll find VFDs in many consumer applications.

LCDs, on the other hand, lend themselves to portable instruments and devices that operate at low power

THE BUS ARCHITECTURE CAREER COMPATIBILITY TEST.

common outputs and 24 segment outputs let you control as many as 12 8-segment digits or eight 9-segment symbols. Before the information display occurs, you store the needed segment patterns in a byte-address area in RAM. μ Cs provide for, let you generate a series of that vary from 0 to almost 100% duty cycle. For example, the 8096 provides any one of 256 duty

cycles, according to the value you put in the timing register. The PWM circuit has a prescaler when you clock the 8096 at 12 MHz. In this approach, Mitsubishi's M50753 uses two prescalers to produce a PWM output. The timers generate on and off times, so you can select the duty cycle and frequency with 8-bit accuracy. By providing a low-pass filter or integrator, you can use the PWM to generate an analog voltage. Another timing function involves a watchdog timer which provides a graceful way of recovery

Strategic issues influence μ C choices

If you've defined your application problem and set up a realistic development timetable—many engineers ignore your μ C choices by examining the chips that come off the assembly line. Although your needs. Although examination sounds obvious, many engineers simply choose the same μ Cs used by their competitors, or they choose the most familiar with. At the extreme, don't try to select a μ C chip on the

chips, examine the depth and breadth of a manufacturer's product line. With few exceptions, most μ C manufacturers offer many chips that contain a variety of I/O ports, memory configurations, timers, serial ports, and additional features. Other manufacturers may provide a few highly specialized chips for narrow markets.

A variety of development tools lets you decide how to tackle a μ C design project. Manufacturers offer plug-in development aids that take the place of the μ C, stand-alone development boards, complete hardware-developed software tools. Manufacturers rally to the IBM PC or compatible computers as hosts for μ C development software. Most μ C suppliers also offer PC-based development tools that start at about \$2500. Third-party vendors also provide development systems and software tools. Besides the availability of software and hardware, check the availability of alternate μ C-chip sources. Many manufacturers now have excess production capacity; by selecting a spe-

cial chip from one source, chip supply may slow when demand picks up again. Also, on a manufacturer's field support port. Engineering support ranges from field engineers can give on-site assistance to one or two engineers in a manufacturing office.

Concern about support includes testability. Because circuits are concentrated—and inaccessible—in the μ C chip, testing can be difficult. Motorola provides self-checking routines within its 6805 and 6811 families. The routines require some external circuits to give a visual indication that the chip works properly. The test routines check I/O ports, timer, counter, ROM, RAM, and CPU. The routines also test an auxiliary counter or an A/D converter if they are on the μ C chip. If you're using a μ C chip that doesn't provide test routines, add them to your code. You'll be adding routines that run product and quality-control tests, so a few additional steps that test the chip's I/O ports, timers, and memory are worth the extra ROM space.

DO YOU ENJOY SPENDING NIGHTS AND WEEKENDS ALONE CONFIGURING YOUR SYSTEM?

<i>Career Compatibility Test</i>			
<i>Bus Capability</i>	<i>VME*</i>	<i>MB II</i>	<i>Mark Your Preference</i>
<i>Geographic Addressing</i>		X	
<i>Built-in Self-Test</i>		X	
<i>Software Configurability</i>		X	

Do you enjoy hunting down a misplaced or missing jumper at 2 o'clock Saturday morning?

If so, don't choose the MULTIBUS[®] II architecture.

Because the MULTIBUS II architecture has an exclusive feature that reduces or eliminates jumpers and dip switches.

It's called geographic

addressing. And it allows boards to be addressed by slot number in software, which eliminates or greatly reduces jumpers. For example, there are no jumpers on the entire line of MULTIBUS II memory boards.

But if you do need jumpers, geographic addressing can still help. Because software can use it to verify correct jumper placement.

And not only is board configuration fully supported in software, but so is identification of board type, manufacturer and the revision level of both hardware and firmware. Geographic addressing also provides a capability for built-in self-test and remote system diagnostics.

Making things a lot easier for you. And resulting in lower test costs and improved serviceability.

But, by all means, if you enjoy tearing your hair out while re-reading the manual for the umpteenth time, catch the other bus.

It doesn't have geographic addressing, so you could find yourself knee deep in jumper and testing problems. Which means you'll spend many long, gratifying nights working at your bench.

Now, indicate your bus choice in the preference box and turn the page.

*Source: IEEE P1014 Draft 1.2, August 1985.
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Choose A/D converters with care—several require external S/H amplifiers.

software or hardware error. A watchdog timer includes a counter circuit that operates independent of the software. When the counter reaches its maximum count and overflows, it generates a signal that resets the CPU. To prevent the counter from overflowing, your software must periodically reset the counter. Should your hardware or software fail and not reset the counter, the counter overflows and resets the computer to provide a fresh start.

Watchdog timers aren't panaceas for hardware and software troubles, however. In fact, they can cause problems if you apply them indiscriminately while performing software and hardware work. For example, if you enable the software timer and your software fails, you'll have a difficult time locating the fault. The watchdog timer periodically resets the CPU and puts the computer in a reset-timeout loop that's difficult to troubleshoot. If you decide to choose a μ C chip that includes a watchdog timer, be sure you can leave it disabled until you need it.

Most μ Cs reset the watchdog timer until you enable it via software. For example, Intel's 8096 manual makes it clear that a reset operation disables the watchdog timer until you enable it. Because the 8096 μ C's watchdog timer includes an overflow flip-flop and a pull-down transistor, the watchdog timer's overflow action resets all external circuits attached to the 8096's RESET line. Don't attempt to override the RESET output for more than a second or two. Because the output transistor can sink 30 mA at 2.0V, you can get localized chip heating that causes unreliable μ C operation. Intel provides several typical reset circuits for the 8096 μ C chip.

NEC's μ PD7809 data sheet isn't clear about when or how you enable the watchdog timer. In practice, the μ PD7809's watchdog timer remains disabled until you enable it by writing to the watchdog-timer register. Once you enable the watchdog timer, you can't disable it unless you reset the μ C chip with an external reset signal.

Clocks govern internal operations

A/D-conversion speeds, serial transmission rates, and other time-related operations depend on the μ C's clock frequency. The chips include an oscillator circuit and thus require only an external quartz crystal or a ceramic resonator to complete the clock circuit (Fig 6). You can use an external clock signal to drive the μ C as long as the clock signal's frequency meets the μ C's requirements. Clock circuits usually require an external buffer that drives one of the crystal input lines. The

Zilog Z8 is an exception—it requires two buffers that drive the crystal input lines out of phase with each other (Fig 7). Keep in mind that manufacturers often specify exact operating frequencies so that internal clock and timer circuits provide standard serial-transmission rates. If you decide to use an external clock, check the UART's specifications to be sure you get the transmission rates you need.

Although NMOS μ Cs operate within a narrow frequency range, their CMOS counterparts can operate at frequencies as low as 0 Hz. As the operating frequency of the CMOS chips decreases, so does their power consumption. The CMOS chips have two other advantages over NMOS devices: CMOS provides greater noise immunity and you can operate the chips over a wide voltage range. RCA's CDP1804AC, for example, operates over 4 to 6.5V and Texas Instruments' TMS70C00 operates between 3 and 5.5V. Typical NMOS μ C chips operate with supply voltages between 4.5 and 5.5V.

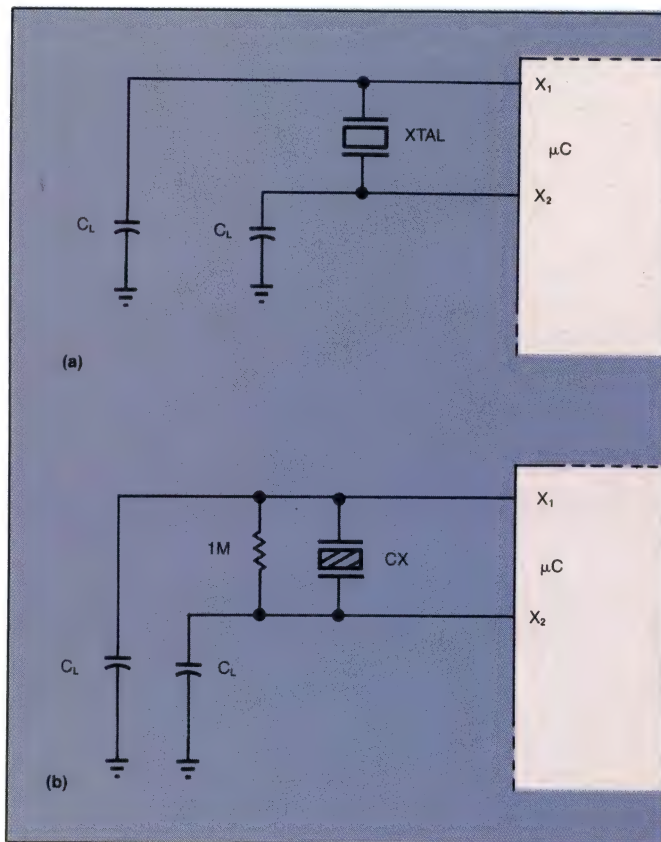


Fig 6—One-chip μ Cs allow direct crystal connections with the internal oscillator circuits (a). As an alternative to a crystal, you can use a less expensive ceramic resonator (b).

DO YOU LIKE THE CHALLENGE OF RELIABILITY PROBLEMS?

<i>Career Compatibility Test</i>			
<i>Bus Capability</i>	<i>VME*</i>	<i>MB II</i>	<i>Mark Your Preference</i>
<i>Power and Ground Pins (PI Connector)</i>	14	30	
<i>Synchronous Protocol</i>		X	
<i>Bus Parity</i>		X	

Somebody switches on a compressor and your computer system dies.

Swell. Is that the kind of career challenge you got into the systems design business for?

If so, don't choose the MULTIBUS® II architecture. Because MULTIBUS II systems ensure reliability in three ways.

First, a large number of power and ground pins provides superior signal quality. Then synchronous protocol gives you increased noise immunity. And protects you from metastability problems.

Finally, bus parity protects against disturbances on any line. Whether it's address, data or control.

On the other hand, if dealing with reliability problems gets your blood pumping, the other bus should give you plenty of satisfying excitement.

It has only 14 power and ground pins compared to 30 on the MULTIBUS II boards. And it doesn't offer you the protection of synchronous operation or bus parity. Which means metastability becomes something to watch out for. The other bus can be very challenging indeed.

Indicate your preference and continue.

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Special serial protocols let μ C and peripheral chips communicate over two or three wires.

Short of controlling a CMOS μ C's clock, you can force many processors into a power-conserving mode when they're waiting for an external event or not processing data. The low-power modes don't turn off the processor, but they put it in an idle state, maintaining the information in internal registers, flags, and RAM. For example, you can halt National Semiconductor's COP210C/211C μ C by including a halt instruction in your program. You can also configure a clock input as an external switch that forces the computer into a halt mode. With the chip in the halt state, power consumption is at its minimum. In addition, the CMOS μ Cs aren't much more expensive than NMOS chips. For example, General Instrument's PIC16C58 costs less than \$2 (100,000).

The Hitachi CMOS HD63705 family provides three low-power or power-down modes: wait, stop, and standby. In the wait mode, the CPU stops processing data but the interrupts and clocks are still active. The stop mode stops the internal oscillator and clears several

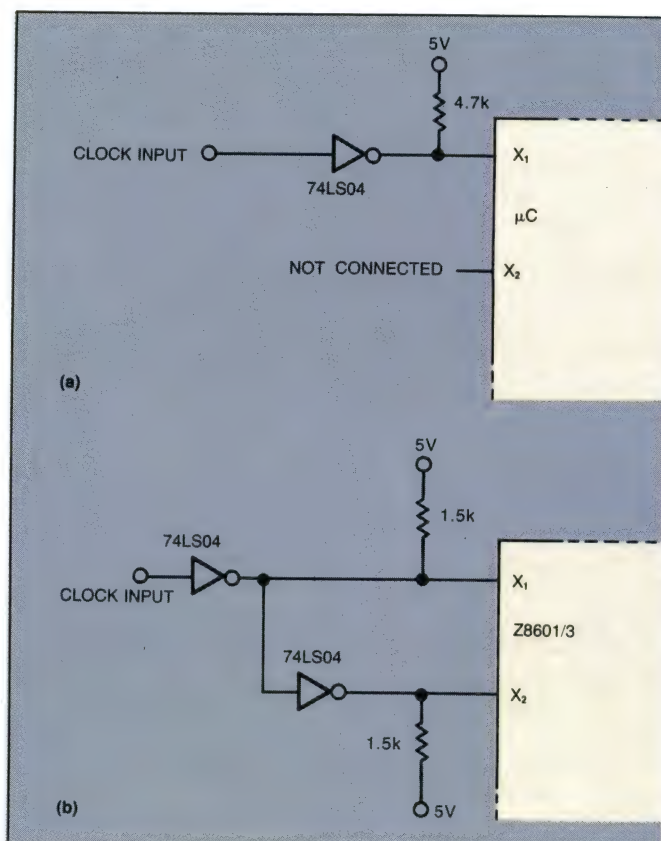


Fig 7—External oscillators drive μ C chips directly (a), but you'll need to use a set of inverting buffers to drive both crystal inputs on the Zilog Z8 μ C chip (b).

Manufacturers of Enhanced 1-chip μ Cs

For more information on enhanced 1-chip μ Cs, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

Advanced Micro Devices Inc
901 Thompson Pl
Sunnyvale, CA 94088
(408) 732-2400
Circle No 689

Fujitsu Microelectronics Inc
3320 Scott Blvd
Santa Clara, CA 95054
(408) 727-1700
Circle No 690

General Instrument Corp
Microelectronics Div
600 W John St
Hicksville, NY 11802
(516) 933-3229
Circle No 691

GTE Microcircuits Div
2000 W 14th St
Tempe, AZ 85281
(602) 968-4431
Circle No 692

Hitachi America Ltd
2210 O'Toole Ave
San Jose, CA 95131
(408) 942-1500
Circle No 693

Intel Corp
3065 Bowers Ave
Santa Clara, CA 95051
(408) 987-8080
Circle No 694

Mitsubishi Electronics America Ltd
Semiconductor Div
777 N Pastoria Ave
Sunnyvale, CA 94086
(408) 730-5900
Circle No 695

Motorola Semiconductor Products
Microprocessor Group
6501 William Cannon Dr W
Austin, TX 78735
(512) 440-2990
Circle No 696

National Semiconductor Corp
2900 Semiconductor Dr
Santa Clara, CA 95051
(408) 721-5000
Circle No 697

NCR Corp
Microelectronics Div
8181 Byers Rd
Miamisburg, OH 45342
(513) 866-7217
Circle No 698

NEC Electronics Inc
401 Ellis St
Mountain View, CA 94039
(415) 960-6000
Circle No 699

Oki Semiconductor Inc
650 N Mary Ave
Sunnyvale, CA 94086
(408) 720-1900
Circle No 700

RCA Solid State Div
Box 3200
Somerville, NJ 08876
(201) 685-6000
Circle No 701

Rockwell International
Semiconductor Products Div
4311 Jamboree Rd
Newport Beach, CA 92658
(714) 833-4700
Circle No 702

Seeq Technology Inc
1849 Fortune Dr
San Jose, CA 95131
(408) 942-1990
Circle No 703

SGS Semiconductor Corp
1000 E Bell Rd
Phoenix, AZ 85022
(602) 867-6100
Circle No 704

Sharp Electronics Corp
10 Sharp Plaza
Paramus, NJ 07652
(201) 265-5600
Circle No 705

Siemens Corp
186 Wood Avenue S
Iselin, NJ 08830
(201) 321-3400
Circle No 706

Signetics Corp
Box 409
Sunnyvale, CA 94086
(408) 739-7700
Circle No 707

Texas Instruments Inc
Semiconductor Group (SC-517)
Box 809066
Dallas, TX 75380
(800) 232-3200
Circle No 708

Toshiba America Inc
2441 Michelle Dr
Tustin, CA 92680
(714) 730-5000
Circle No 709

Zilog Inc
1315 Dell Ave
Campbell, CA 95008
(408) 370-8000
Circle No 710

DO YOU CHERISH MULTIPROCESSING LIMITATIONS?

<i>Career Compatibility Test</i>			
<i>Bus Capability</i>	<i>VME*</i>	<i>MB II</i>	<i>Mark Your Preference</i>
<i>Virtual Interrupts</i>		X	
<i>Number of Interrupt Levels</i>	7	255	
<i>Distributed Arbitration</i>		X	
<i>Number of Arbitration Levels</i>	4	20	

Does the anguish of running out of interrupts give you a masochistic sense of pleasure?

If so, stay away from the MULTIBUS® II architecture.

Because of its virtual interrupt feature, MULTIBUS II boards give you all the sources and destinations of interrupt you need for multiprocessing. Up to 255.

And to make it an even stronger candidate for

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Of course, if you believe that needless frustration builds character, you should choose the other bus.

You'll be stuck with a dedicated interrupt arrangement that effectively allows you only seven interrupts. And because it uses central arbitration, you're effectively limited to only four masters.

Of course, if you want to design systems that are more powerful, useful and flexible, you should choose the MULTIBUS II architecture.

Now turn to the last page and complete the test.

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register bits but doesn't affect the internal RAM. You should save register information in RAM and restore the registers as you leave the stop mode. In its standby mode, the HD63705 maintains data in the internal RAM, but it clears all internal registers.

The RCA CDP6805E2 μ C dissipates 35 mW at full speed when operated from a 5V power supply. The chip's wait and stop modes dissipate 5 mW and 5 μ W, respectively. On the other hand, a typical 8051 NMOS μ C chip dissipates 800 mW. Keep in mind that clock frequency affects CMOS power dissipation. The higher the clock's frequency, the more power the CMOS μ C chip uses. Power requirements for NMOS μ C chips don't vary with respect to clock frequency, and NMOS μ Cs operate within a narrow clock-frequency range.

Saving information is important, particularly in case of power failure, so several μ Cs provide RAM backup. SGS Semiconductor's M38SH72 contains 64 bytes of RAM in the main memory space. When power is lost, the μ C writes the 64 bytes of RAM into a nonvolatile shadow RAM. Applying power causes the CPU to place the shadow RAM's contents back in the 64 bytes of main RAM. Such chips as Intel's 8096, SGS's M3875, and Toshiba's TLCS-4 family operate with a battery backup for internal RAM. The amount of battery-powered RAM varies; the 8096 backs up 16 bytes and the M3875 backs up all 64 bytes.

EDN

Article Interest Quotient (Circle One)
High 470 Medium 471 Low 472

DO YOU THINK GUARANTEED COMPATIBILITY IS FOR SISSIES?

<i>Career Compatibility Test</i>			
<i>Bus Capability</i>	<i>VME*</i>	<i>MB II</i>	<i>Mark Your Preference</i>
<i>Synchronous Protocol</i>		<i>X</i>	
<i>Spec Options</i>	<i>Many</i>	<i>Few</i>	

When a board from manufacturer X doesn't work with a board from manufacturer Y, do you secretly get a perverse sense of delight?

If so, you won't be happy with the MULTIBUS® II architecture.

Since it has a synchronous protocol. Which not only provides noise immunity, but compatibility as well.

In fact, synchronous

protocol, because of the very rigorous definition it requires in specs, virtually guarantees compatibility among MULTIBUS II boards from different vendors. And across many generations of VLSI. Assuring a long life for your products.

The other bus has a very unconstrained asynchronous protocol. With lots of spec options. Which gives board manufacturers lots of "leeway." So all sorts of delightfully unpredictable things can happen. For instance, bus timing can change when boards are added or removed from the backplane. Signal edge rates can change too. And options can lead to incompatibilities.

Of course, maybe you think putting up with that kind of frustration is what you trade for higher performance.

Not so. The MULTIBUS II architecture can run faster than the other bus.

So mark your preference now. We'll wait. Then put your pencil down because this is the end of the test.

If you chose the MULTIBUS II architecture more often, read on. If you chose the other bus more often, you might consider a new career direction (or a good course in stress management).

Still with us? Good. Want to learn more? Then call or write for our MULTIBUS II Technical Series: Intel Corporation, Lit. Dept. W262, 3065 Bowers Ave., Santa Clara, CA 95051.

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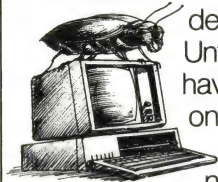
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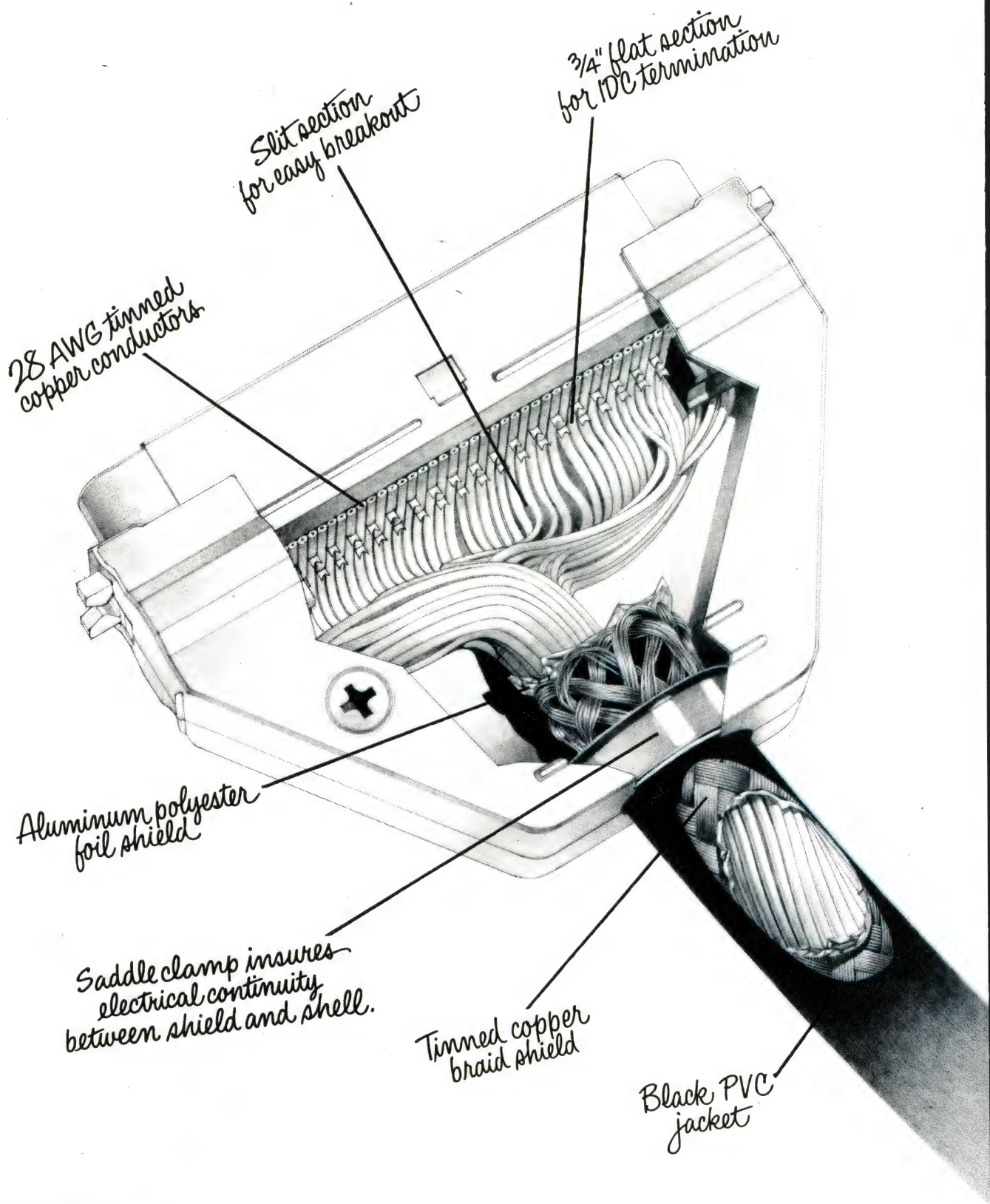
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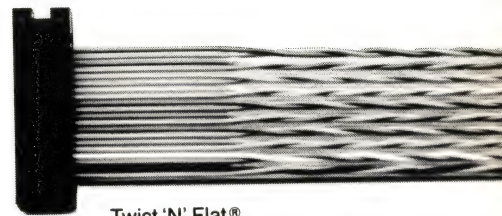
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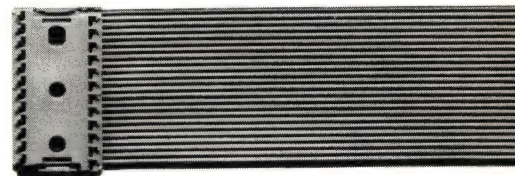
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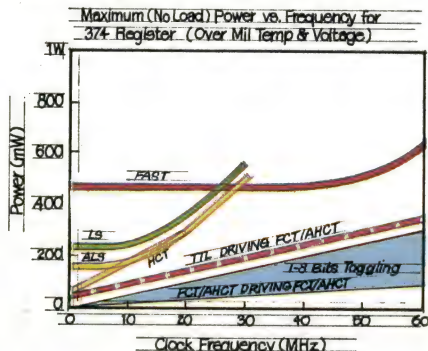
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Mil AHCT = 12mA

IDT54/74 FCT and AHCT

Introduction

Registers

374	Now
273	Now
299	Now
377	Now
534	Now

Latches

373	Now
533	Now

Buffers

240	Now
244	Now

Transceivers

245	Now
645	Now
640	Now

Decoders

138	Now
139	Now

Comparators

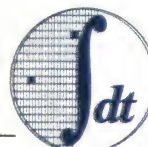
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Floating-point math handles iterative and recursive algorithms

Floating-point arithmetic gives you better dynamic range and precision than integer arithmetic, but it needs careful implementation. Part 1 of this 3-part series discusses possible sources of error you may encounter when using floating-point hardware, and it reviews the current standards. Part 2 will describe the advantages of fast array processors, and part 3 will discuss algorithmic options for floating-point processors and considerations when implementing a complete system.

Charlie Ashton, *Advanced Micro Devices Inc*

Many signal-processing algorithms, such as fast Fourier transforms, generate outputs whose magnitudes far exceed those of the inputs. Nevertheless, those outputs must retain the precision of the input operands if the accuracy of the computation is not to be so severely degraded as to render the results meaningless. For these and similar applications that use iterative or recursive algorithms, true floating-point operation often furnishes the only acceptable number representation.

Until recently, you needed a very good reason to give

your system floating-point hardware. It was large, expensive, power-hungry, and relatively slow (although faster than the software-based implementations needed to perform comparable operations). However, the introduction of fast VLSI array processors has changed the picture. These devices (such as Weitek's 1032/1033 and AMD's Am29325) can stand alone and are implemented on one or two chips. You can now economically use floating-point hardware in applications whose size and budget constraints would previously have forced the use of fixed-point hardware or floating-point software.

The new chips won't dissipate all your potential headaches, of course. Just one of the many choices you'll have to make is which standard to support. The four most commonly used standards (IEEE, DEC, IBM, and MIL-STD-1750A) have subtly different binary representations of floating-point numbers. Each standard has advantages and disadvantages for specific types of computational problems. This series of articles covers some of the theoretical considerations you'll have to take into account, as well as some specifics on the available chips.

The manner in which a system represents floating-point numbers clearly affects both the dynamic range and the precision of the system. The most obvious way

VLSI processors now make floating-point hardware cost effective in applications with severe budget or size constraints.

to represent numbers is to use a signed exponent and a signed fraction (Table 1). A large exponent field obviously supports a large dynamic range: A 2-digit exponent, for example, implies a dynamic range of 10^{100} , whereas a 3-digit exponent increases the dynamic range to 10^{1000} . Similarly, the more digits you can include in the fraction, the greater will be the precision of the number, especially if the number is normalized so that the left-most digit of the fraction is nonzero. Leading zeros in the fraction of an unnormalized number clearly reduce the precision of that number. As a general principle, then, the precision of a floating-point

TABLE 1—SIGNED vs BIASED EXPONENTS

DECIMAL NUMBER		SIGNED EXPONENT		FRACTION
-123.45	=	10^{-3}	x	-0.12345
+0.0000678	=	10^{-4}	x	0.678

DECIMAL NUMBER		BIASED EXPONENT		FRACTION
-123.45	=	$5+3=8$	x	0.12345
+0.0000678	=	$5-4=1$	x	0.678

number depends on the length of its fraction, and the dynamic range depends on the size of the exponent and the radix.

In practice, floating-point hardware generally uses a biased exponent for two reasons. First, use of a biased exponent avoids problems that follow from the need to handle negative numbers in the exponent circuitry. Second (and perhaps more important), a suitable choice of bias can ensure that you'll be able to compute the reciprocals of all the representable numbers without exponential overflow or underflow. You'll find that overflow and underflow cause plenty of problems in computing the fraction portion of the output (see **box**, "Dealing with underflow and overflow"). You certainly don't want to introduce them into exponential computations as well.

Biased exponents and normalized fractions are the features that give true floating-point representation a clear advantage over block floating-point and integer formats. To double the dynamic range of an integer word, you have to double the number of bits in it. To obtain the same result in true floating-point operation, you need to add only one bit to the exponential field. In

fact, a 32-bit floating-point number in IEEE format has a dynamic range equivalent to that of a 276-bit 2's-complement integer.

Despite the high precision and large dynamic range of normalized floating-point numbers, floating-point systems do not altogether escape the effect of quantization (rounding) errors. You can think of a floating-point system as producing an infinitely precise result (ie, a fraction of unlimited length, abbreviated "IPR"), which is then rounded to fit into the destination format. Typically, this strategy means that some of the low-order fraction bits are lost. Consequently, whenever the destination format lacks enough bits to accommodate the IPR, rounding introduces quantization errors, which in turn result in system noise. Consider, for example, the multiplication of two numbers in a 4-digit decimal system:

$$(0.8102 \times 10^3) \times (0.8001 \times 10^{-7}) = 0.6410401 \times 10^{-4}.$$

The IPR is rounded to 0.6410×10^{-4} to fit the destination format, thus introducing a quantization error. In practice, quantization errors during a long computation will be random, and the overall effect will be analogous to an increase in system white noise. If the quantization errors are *not* random, they may appear as system nonlinearities and, as a consequence, cause serious problems in such applications as spectral analysis.

Are quantization errors data dependent?

Mathematical analysis of an integer system shows that quantization errors due to rounding have a mean value of one-quarter the value of the least significant bit. The relative error at each rounding thus depends on the magnitude of the operand being rounded. Therefore, as the magnitude of the operand decreases, the relative quantization error increases. The same is true of a block floating-point system, in which denormalized operands may contain leading zeros. In integer and block-floating-point systems, therefore, the errors are data-dependent, and for this reason error analysis is both difficult and time-consuming.

In true floating-point systems, however, operands are generally normalized, so the relative quantization errors are the same, regardless of the magnitude of the operands. Quantization error analysis in floating-point systems is thus data independent and therefore doesn't require complicated worst-case simulations.

Floating-point systems can suffer from a computational drawback known as the "operand ordering prob-

lem." Consider the addition of three floating-point numbers: $A (=1)$, $B (=2^{90})$, and $C (= -2^{90})$. You may find that $(A+B)+C=0$, although $A+(B+C)=1$. This result clearly violates the associative law of addition. The discrepancy occurs because the floating-point standard doesn't have enough bits to accommodate the intermediate result of the first calculation $(A+B)$. The hardware has to round the IPR, $2^{90}+1$, to the nearest representable number, which is 2^{90} . Errors of this kind are inevitable whenever the IPR has to be rounded to fit the destination format, although they would usually be considered so small as to be unimportant.

You can minimize rounding errors (although, as the previous example shows, you can't entirely remove them) by a judicious choice of rounding mode. Some floating-point standards allow you to select from among several rounding modes the one that best suits your operation. All of the commonly used floating-point standards support one or more of four modes:

- Round-to-nearest mode replaces the IPR with the closest representation that fits in the destination format. In the case of an IPR that falls exactly halfway between two representations, the IEEE standard rounds the IPR to the representation

Dealing with underflow and overflow

For the rare cases in which the result of a calculation is too large or too small to be represented, you must have previously specified the way in which your system will deal with that result. In short, your system must handle the related problems of underflow and overflow.

Underflow arises when the rounded result of an operation is a number between zero and the smallest representable normalized number. You can handle such a number in one of two ways: You can set the number to zero (sudden underflow), or you can represent the rounded result by a denormalized number (gradual underflow).

Overflow occurs when the rounded result of an operation is greater than the largest representable number. You can handle this problem by setting the result to infinity, which implicitly terminates a chain of calculations, or by saturating the result to the largest representable number (correctly signed).

It's important to know which of the various methods your system supports, because in some

applications sudden underflow or saturated overflow can destroy the accuracy of an entire series of calculations. The IEEE standard, for example, treats underflows by invoking the gradual underflow method, while the IBM and DEC standards deal with only sudden underflow.

Sudden underflow is generally the fastest method of treating underflows and is acceptable in the majority of systems because high accuracy is seldom required for very small numbers. Sudden underflow can produce quantization errors almost as large as the smallest normalized number, but usually you can treat these errors as insignificant.

The gradual-underflow method creates much smaller errors because it rounds results to a normalized number. On the other hand, gradual underflow is more difficult and more expensive to implement than sudden underflow, a drawback you'll have to weigh against the advantage of accurate results over a wider range of numbers. Gradual underflow is generally best for iterative applications in which

you drive a residual value to zero and for which you require maximum possible accuracy. When such a residual value underflows gradually to zero, you know that it's negligible compared with every normalized number.

For handling overflow, data-processing applications generally set the result to infinity, because in a high-accuracy mathematical model a saturated result could destroy the accuracy of an entire series of calculations. In real-time digital signal processing, however, it's generally preferable to saturate the result and continue the chain of calculations. In the analysis of radar returns, for example, you would certainly not want a single anomalous return to bring the entire processing sequence to a halt by introducing an operand (an infinity) that would be useless in further processing. In this and similar applications, it's often better to have an approximately correct data point than no data point at all.

TABLE 2—NUMBER REPRESENTATION IN FOUR FLOATING-POINT STANDARDS

IEEE FORMAT

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	3	2	1	0
	S	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-20}	2^{-21}	2^{-22}	2^{-23}
	SIGN	BIASED EXPONENT								FRACTION							
	S	(E)								(F)							

$E = 0$ AND $F = 0$ $V = (-1)^S * 0 (-0, +0)$
 $E = 0$ AND $F \neq 0$ $V = (-1)^S * 0.F * 2^{-126}$ (DENORMALIZED)
 $0 < E < 255$ $V = (-1)^S * 1.F * 2^{E-127}$ (NORMALIZED)
 $E = 255$ AND $F = 0$ $V = (-1)^S * 00 (-\infty, +\infty)$
 $E = 255$ AND $F \neq 0$ $V = \text{NaN (NOT-A-NUMBER)}$

(a)

DEC FORMAT

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	3	2	1	0
	S	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-21}	2^{-22}	2^{-23}	2^{-24}
	SIGN	BIASED EXPONENT								FRACTION							
	S	(E)								(F)							

$S = 1$ AND $E = 0$ $V = \text{DEC RESERVED OPERAND}$
 $S = 0$ AND $E = 0$ $V = 0$
 $E > 0$ $V = (-1)^S * 0.1F * 2^{E-128}$ (NORMALIZED)

(b)

IBM FORMAT

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	3	2	1	0
	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-21}	2^{-22}	2^{-23}	2^{-24}
	SIGN	BIASED EXPONENT								FRACTION							
	S	(E)								(F)							

$F = 0$ $V = (-1)^S * 0 (-0, +0)$
 $F \neq 0$ $V = (-1)^S * 0.F * 16^{E-64}$

(c)

MIL-STD-1750A FORMAT

BIT	31	30	29	28	27		11	10	9	8		7	6	5	4	3	2	1	0	
	-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	...	2^{-20}	2^{-21}	2^{-22}	2^{-23}		-2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	
	FRACTION										EXPONENT									
	(F)										(E)									

..... $V = F * 2^E$

(d)

Biased exponents and normalized fractions give true floating-point systems a clear advantage over integer and block-floating-point systems.

having an LSB of zero, whereas the DEC standard rounds the IPR to the representation that has the greater magnitude.

- Round-to-minus-infinity mode rounds the IPR to the closest representable value that is less than or equal to the IPR.
- Round-to-plus-infinity mode rounds the IPR to the closest representable value that is greater than or equal to the IPR.
- Round-to-zero mode is analogous to truncation; it rounds the IPR to the closest representable value with a magnitude less than or equal to that of the IPR.

As noted earlier, the various floating-point standards specify different binary representations of floating-point numbers, and you'll have to match their respective advantages and disadvantages to your own computational problems. The four of the most common binary floating-point standards, the IEEE, DEC, IBM, and MIL-STD-1750A standards, all represent single-precision, floating-point numbers by means of 32-bit words having the formats shown in **Table 2**. All four standards support double-precision data, and some of these standards also support other data types, such as single-extended and double-extended data.

The IEEE working group presented the specifications contained in proposed standard P754, draft 10.1, as a robust standard for portable floating-point software. This proposed standard has received wide acceptance, and it's likely to form the basis of a large number of future hardware implementations. P754 has

several features that aren't found in other standards. In particular, +0, -0, and infinities are all valid operands. Operations performed on infinities signal no exceptions unless the operation itself is invalid. The standard allows the use of a special operand known as NaN (Not-a-Number). An implementation should interpret NaNs as signals rather than numbers, and it should use NaNs to indicate invalid operations or to pass status information through a series of calculations. Also, the standard accepts denormalized numbers as a representation of a result that is less than the smallest normalized number.

The DEC standard is implemented in all DEC VAX minicomputers; the VAX Architecture Manual contains the full specifications of the standard. Conceptually simpler than the IEEE standard, the DEC standard has no provisions for infinities or denormalized numbers, and it has only a single representation for zero. The DEC standard does, however, incorporate DEC reserved operands, which are analogous to IEEE NaNs.

An important feature common to both the IEEE and the DEC standards is the existence of a hidden bit. Both standards specify that all operands will be normalized (except for denormalized numbers in the IEEE format). This stricture implies that the leading fraction bit must always be a one. This bit would not only be redundant if included in the 32-bit representation, but it would actually reduce the precision of the number, so its presence is assumed. In the case of IEEE denormalized numbers, the biased exponent is zero, thereby

TABLE 3—COMPARISON OF FLOATING-POINT STANDARDS

	IEEE	DEC	IBM	1750A
LARGEST POSITIVE NUMBER	$2^{128} - 2^{104}$	$2^{127} - 2^{103}$	$2^{253} - 2^{228}$	$2^{127} - 2^{103}$
SMALLEST POSITIVE NUMBER	2^{-149}	2^{-128}	2^{-280}	2^{-129}
LARGEST NEGATIVE NUMBER	$-2^{128} + 2^{104}$	$-2^{127} + 2^{103}$	$-2^{253} + 2^{228}$	-2^{127}
SMALLEST NEGATIVE NUMBER	-2^{-149}	-2^{-128}	-2^{-280}	-2^{-129}
DYNAMIC RANGE	2^{277}	2^{255}	2^{533}	2^{256}
PRECISION	2^{-23}	2^{-23}	2^{-20}	2^{-23}

VLSI floating-point μ P for recursive algorithms

One example of floating-point hardware that handles recursive algorithms is the Am29325 from Advanced Micro Devices. The processor integrates a 32-bit adder/subtractor, a multiplier, and a data path on a single chip. This level of integration reduces the processing overhead incurred by chip sets comprising separate ALU and multiplier chips. The internal feedback paths facilitate the implementation of such recursive algorithms as sum-of-products and Newton-Raphson division.

The processor supports both the IEEE and DEC floating-point formats. The instruction set includes instructions that convert data from IEEE format to DEC format and vice versa, as well as instructions that convert data to and from 32-bit integer format.

Three functional blocks

The processor has three main functional blocks (**Fig A**): a floating-point ALU, a status-flag generator, and a 32-bit internal data path. The ALU is fully combinatorial, and it performs all instructions in a single cycle. The eight instructions handle floating-point $R+S$, $R-S$, $R \times S$, and $2-S$ operations as well as the format conversions.

The $2-S$ instruction forms the core of the Newton-Raphson division algorithm, which performs division by a sequence of iterations. In this and other iterative algorithms, intermediate results are retained in the R or S register, thereby eliminating the need for any off-chip registers and minimizing the number of required data transfers.

Three programmable I/O modes allow the Am29325 to interface with a variety of systems. The 32-bit, 2-input-bus mode uses three separate 32-bit

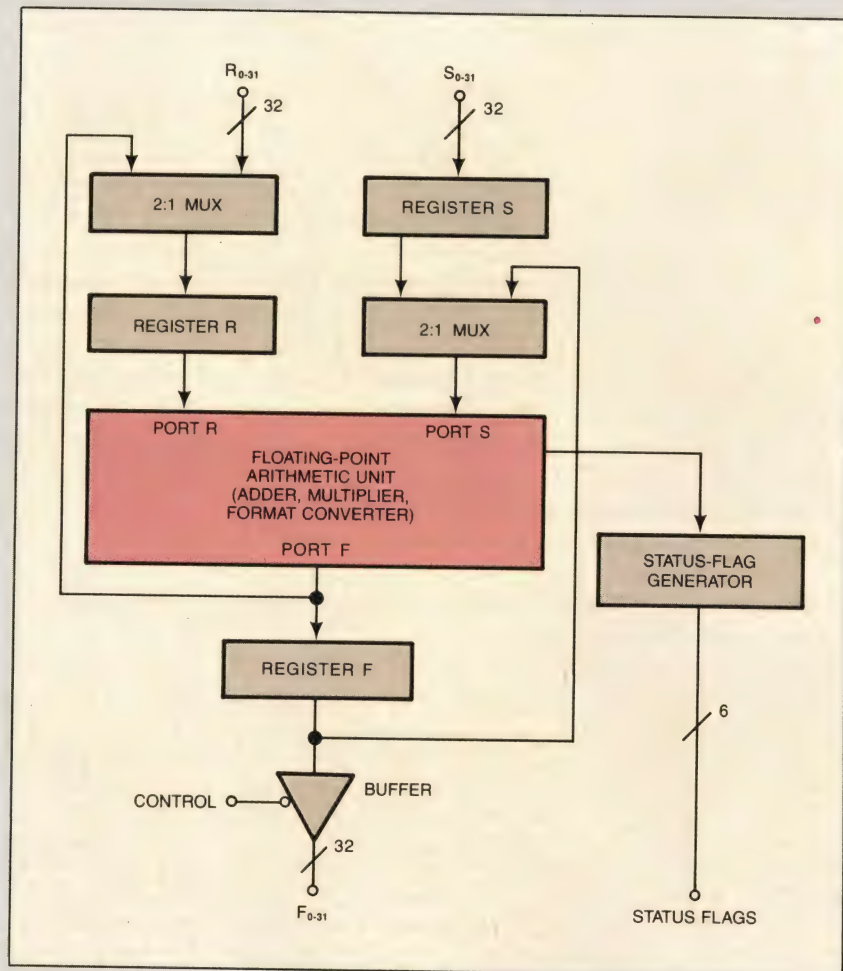


Fig A—This VLSI floating-point processor is fast because it contains all the major components for 32-bit operations on a single chip. It has one input for an external clock and 17 inputs for instruction-select and control functions.

buses (R, S, and F) for high-speed, nonmultiplexed operation; in this case, the R and S registers are configured as independent 32-bit ports. In the 32-bit, 1-input-bus mode, both the R and S registers are connected to a common 32-bit input bus; the host multiplexes operands onto this bus. In the 16-bit, 2-input-bus mode, 32-bit operands are multiplexed onto the corresponding 16-bit buses (low-order bits first).

Six flags and four modes

The status-flag generator provides six fully decoded flags. Four of these flags report exceptional conditions, as defined in

the IEEE standard. The remaining two flags identify zero-valued or nonnumerical results.

The Am29325 implements the four IEEE-mandated rounding modes: round-to-nearest, round-to-plus-infinity, round-to-minus-infinity, and round-to-zero. The same four modes are supported for the DEC standard, except that when the infinitely precise result is halfway between two representable numbers, the IEEE round-to-nearest mode rounds to the closest representation with an LSB of zero, whereas the DEC round-to-nearest mode rounds to the value with the larger magnitude.

instructing the system to assume that the value of the hidden bit is also zero.

The IBM floating-point standard differs from its IEEE and DEC counterparts in several respects. It has no provision for infinities or reserved operands, although it does accept denormalized numbers. More important, however, are the absence of a hidden bit and the use of radix 16 rather than radix 2. Because the exponent of an IBM number is expressed as a power of 16, the standard has a large dynamic range. For the same reason, however, numbers are spaced farther apart than in the other formats. This increased granularity results in less precision than is provided by the IEEE and DEC formats. Also, the use of radix 16 allows as many as three leading zeros in the binary fraction of a normalized number, even though the leading hexadecimal digit is nonzero if the number is expressed in hexadecimal format. The leading binary zeros can cause the precision to vary from one operand to another. This variation is known as wobbling.

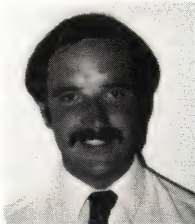
The MIL-STD-1750A standard, developed for use in military systems, allows no reserved operands, infinities, or denormalized numbers. Furthermore, the use of a 2's-complement fraction, rather than a sign-magnitude representation as in the other three formats, requires a somewhat different hardware architecture.

The applications to which each of the four standards is best suited differ quite widely. Nevertheless, you can make a simple comparison (Table 3) between the standards, based on factors such as the largest and smallest representable numbers, the dynamic range, and the precision. Such a comparison can be useful in selecting the most suitable format for a given application. In most cases, however, the format to be used is determined by outside constraints, such as compatibility with existing hardware or software.

EDN

Author's biography

Charlie Ashton is a senior engineer in the product-planning division of Advanced Micro Devices Inc (Sunnyvale, CA). His duties include defining array-processing products. Charlie holds a BSc degree from Reading University, UK, and he is a member of the British IEE. In his spare time, he enjoys cricket, hiking, and swimming.



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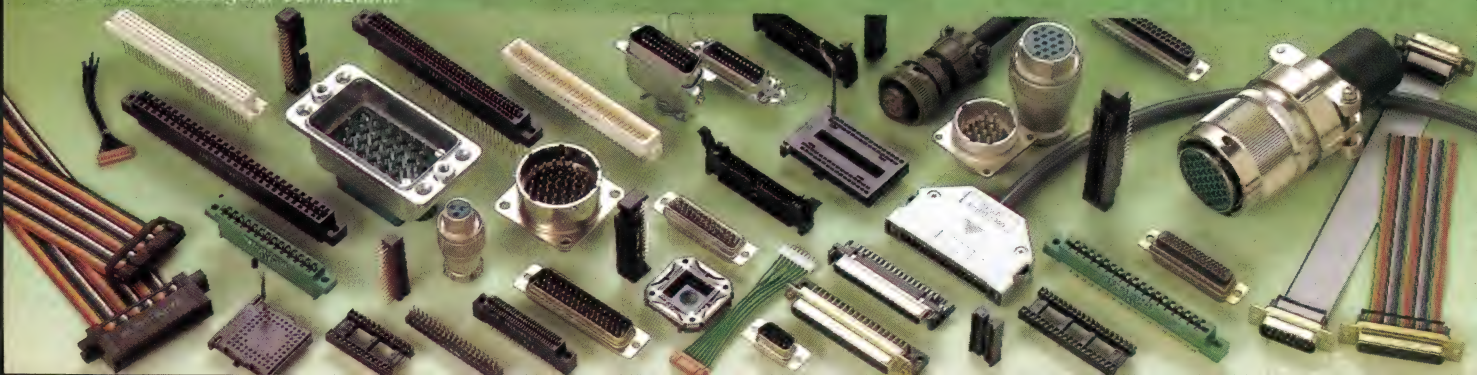
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CIRCLE NO 97



Do your analog circuits live in a noisy neighborhood?

Noise destroys performance in precision analog circuits. Containing it can be a major undertaking.

When a 16-bit system routinely delivers less than 16-bit accuracy, you can probably guess what the problem is.

Noise.

It's the nemesis of sensitive analog circuits.

You probably know the obvious sources of noise like poor grounding, 60 Hz signals from power lines, and spikes from relays and switches. But how about the not-so-obvious causes?

A noise check list.

Here are some considerations.

Are the digital and analog traces located too closely together?
Are the capacitor leads too long?

How about the ground planes? Perhaps they're too small to minimize the radiated signals.

What are the criteria for selecting passive components? Are they chosen by price, by size... or by default? Resistors and capacitors can vary in noise output depending on the materials they're made from and the stresses they operate under.

Now let's look at IC noise. Problems can start with a lack of cleanliness in the manufacturing process, inconsistent diffusion depth and even the layout of the IC itself. There can be significant lot-to-lot variations with some vendors. If you tested only the ICs used in the prototype, you may be in for a surprise later on.

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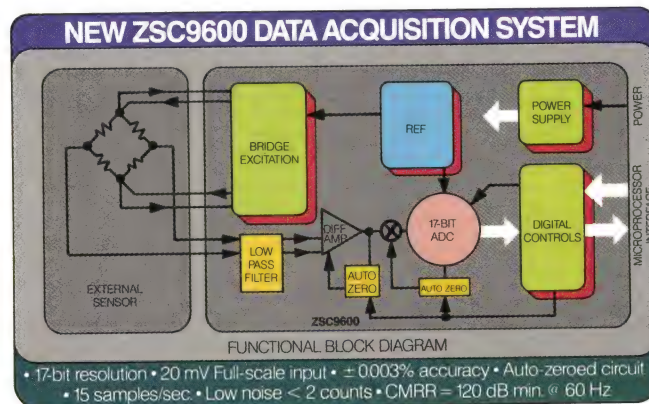
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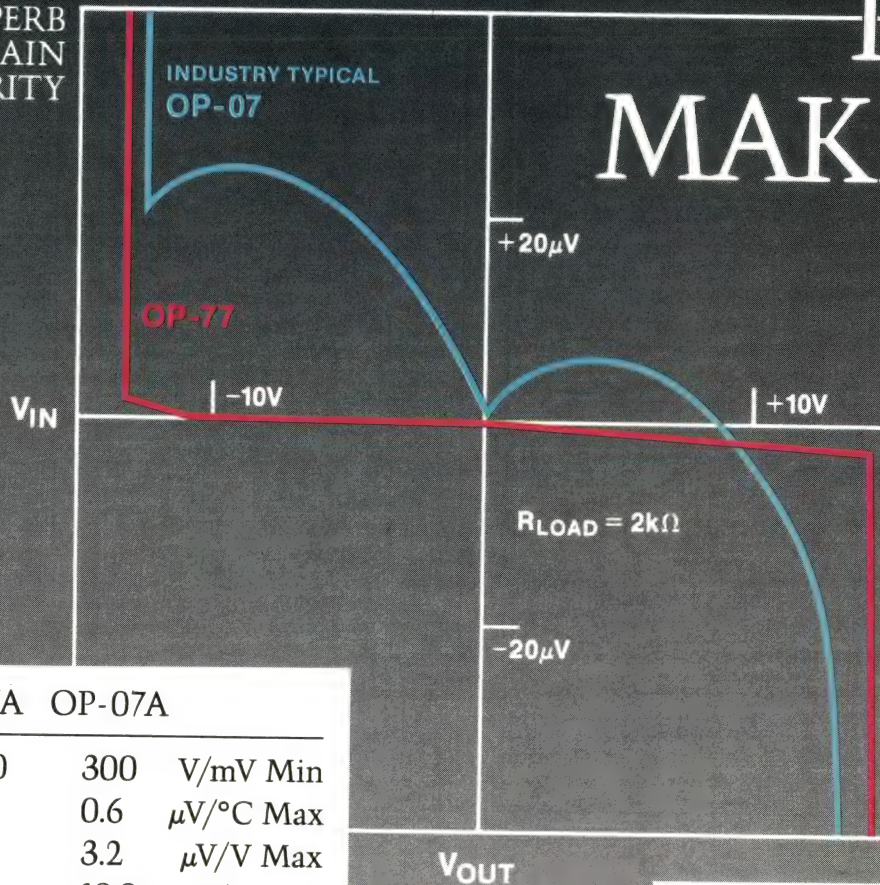
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PSR	3.0	10.0	$\mu V/V$ Max
P_D	60	120	mW Max

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The precision solution.

Test your analog-design IQ

Part 2

Midterm break is over; it's time to test your skill with 25 entirely new linear-design challenges, some of which have deliberately planted bugs. Designed with more recent ICs than those in Part 1, these circuits reflect modern-day speed and stability problems.

Jim Williams, *Linear Technology Corp*

Pit your wits against analog gremlins in this quiz, a continuation of the test that appeared in EDN's Nov 28, 1985, issue. (Part 1 is an updated version of the quiz that appeared in the October 5, 1979, issue of EDN.) These new circuits incorporate more recent semiconductor devices, many of which were unavailable in 1979. The circuits demonstrate the enhanced speeds and stability possible with today's devices.

Ready? Begin!

1. Fig 1 shows a motor-speed control circuit that uses the motor's back EMF as the speed signal. IC₁, configured as an oscillator, drives the Q₁-Q₃ pair, thereby providing pulsed excitation to the motor. The 4016 switch and associated components form a synchronously updated servo amplifier. The speed signal, sampled

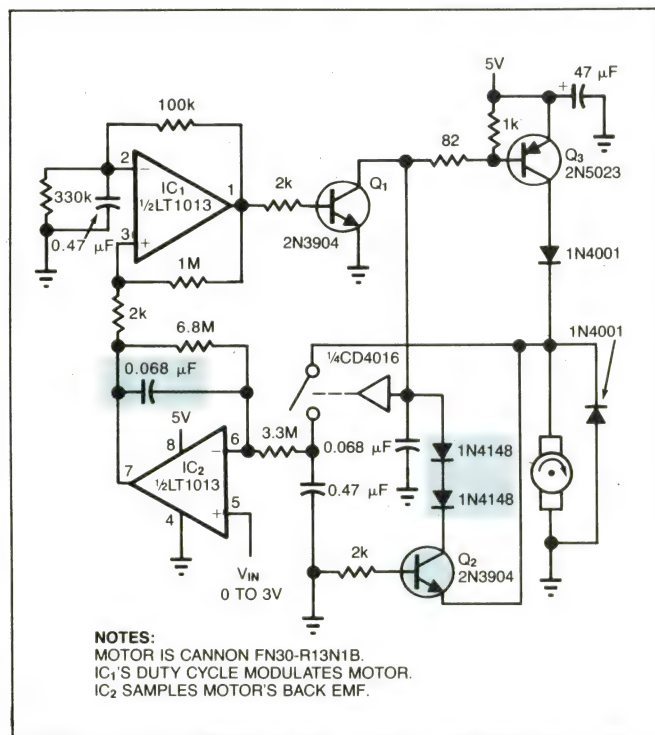


Fig 1—Q₂, the 0.068-µF capacitor, and the 1N4148 diodes in this motor-speed control circuit play a vital role. What is that role?

between Q₃'s output pulses, is stored in the 0.047-µF capacitor. IC₂'s output, a dc signal, closes the loop at IC₁'s noninverting input. IC₁ responds by varying its duty cycle to control motor speed. What are the func-

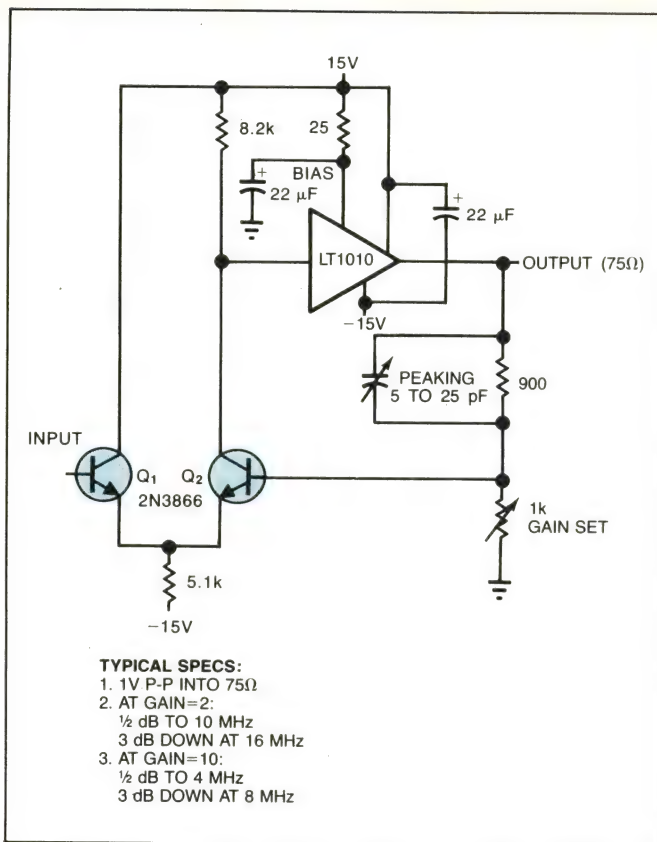


Fig 2—Eliminate the output offset caused by V_{BE} mismatch in the input transistors in this video amplifier.

tions of Q_2 , the $0.068\text{-}\mu\text{F}$ capacitor, and the 1N4148 diodes?

2. The circuit in **Fig 2** is a video amplifier. Although the dc response of video amplifiers is generally not crucial, it's a good idea to minimize offset in the amplifier's output. A mismatch in the V_{BE} s of the discrete input transistors can generate such output offset voltages, particularly at high gains. Suggest a simple way to solve the problem.

3. **Fig 3** shows a quartz-stabilized V/F converter. It operates by clocking the LTC1043 charge pump in such a way as to force the voltage at IC_1 's summing junction to 0V. IC_1 's output ramp sets the flip-flop, and the IC_2 quartz-controlled oscillator resets it. The flip-flop's resultant Q_1 output controls the charge pump. The LM199- IC_3 combination serves as a reference. The circuit's schematic diagram contains two errors. Find them.

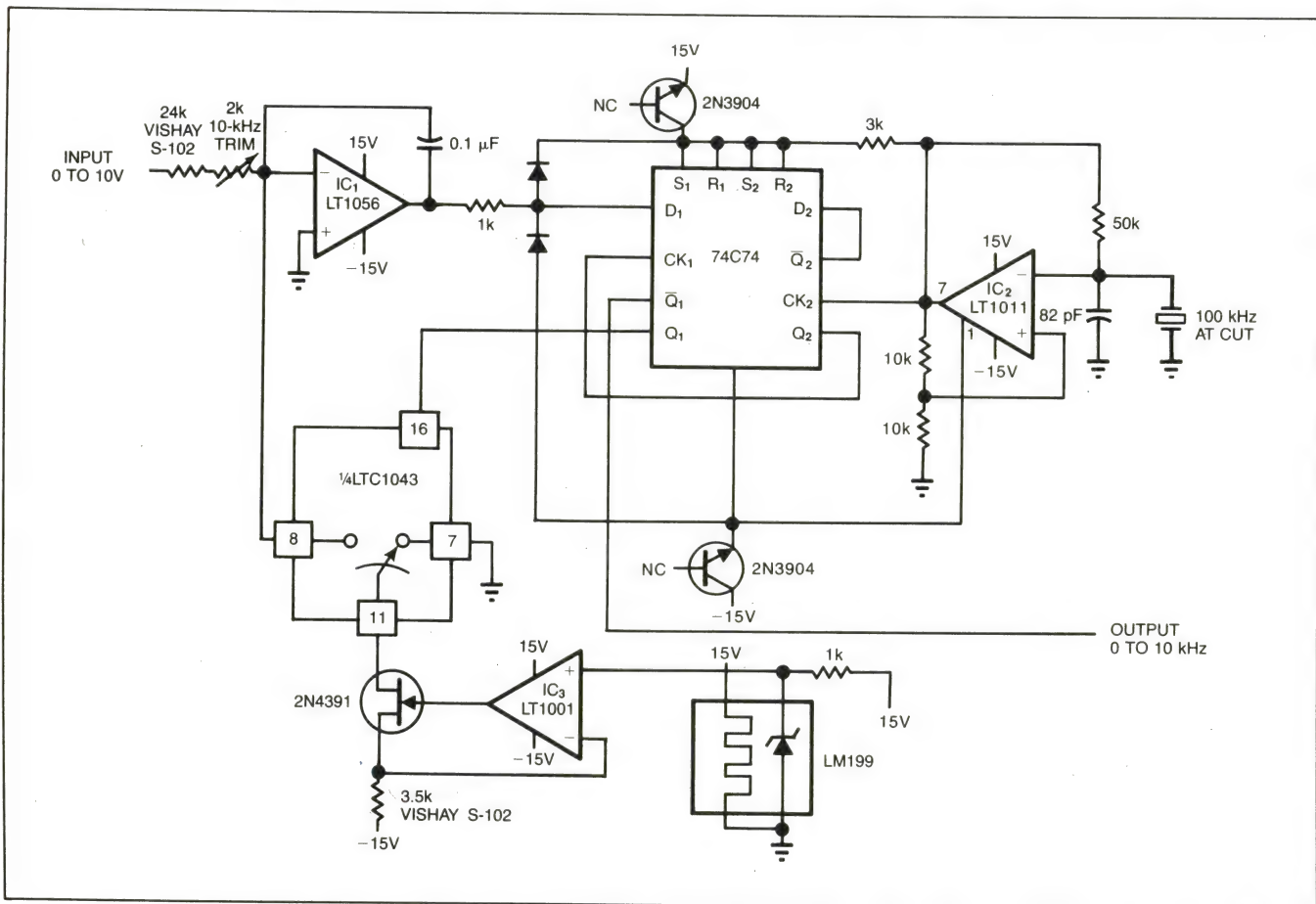


Fig 3—This quartz-stabilized V/F converter won't work. Can you find and correct the two connection errors that prevent this circuit from functioning properly?

You must sometimes use subtle circuit tricks to stabilize or protect linear circuitry.

4. Something is missing from the circuit in **Fig 4**. What is it?

5. **Fig 5** shows a fast level shifter that converts the LT1016's TTL outputs to +5, -10V levels for FET-gate drive. With the addition of two components, the circuit will switch in the 3- to 4-nsec range. Add the necessary components.

6. The crystal-oscillator circuit in **Fig 6** functions well with AT-cut crystals designed to operate at approximately 10 MHz or below. With higher-frequency crystals, however, the circuit often provides multiples of

the intended frequency. Devise a simple solution to the problem and explain why your solution works.

7. The circuit in **Fig 7** is a simple voltage reference. The inverted-mode transistor serves as a first-order, temperature-compensated zener diode, and the op amp provides scaled buffering. The 5-nF capacitor filters noise. Most voltage references of this type work, but some exhibit output noise. There is a very evil gremlin in this circuit. What is it?

8. **Fig 8** gives the schematic diagram of a μ A733 video amplifier. The configuration of the input stage

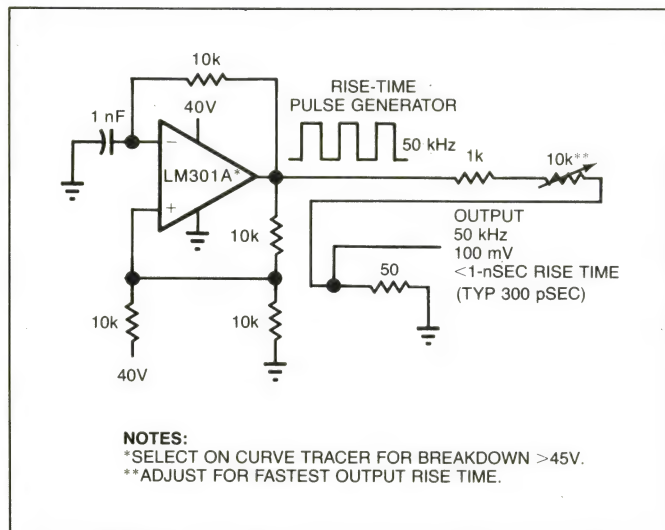


Fig 4—Something is missing from this pulse-generation circuit. What is it?

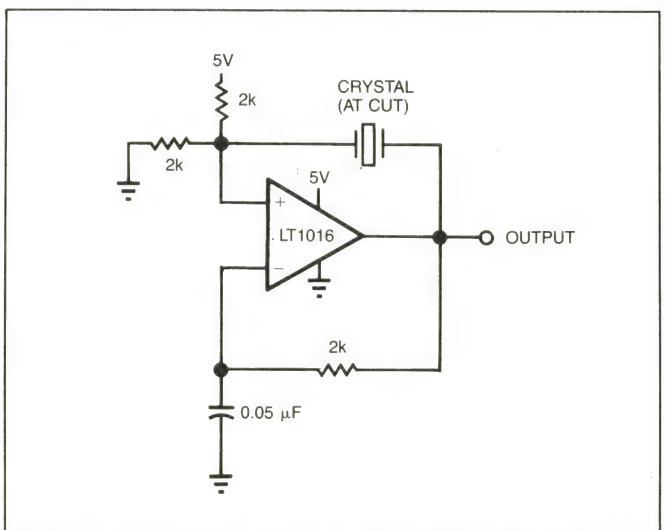


Fig 6—Eliminate the 10-MHz high-frequency limitation inherent in this crystal-oscillator circuit.

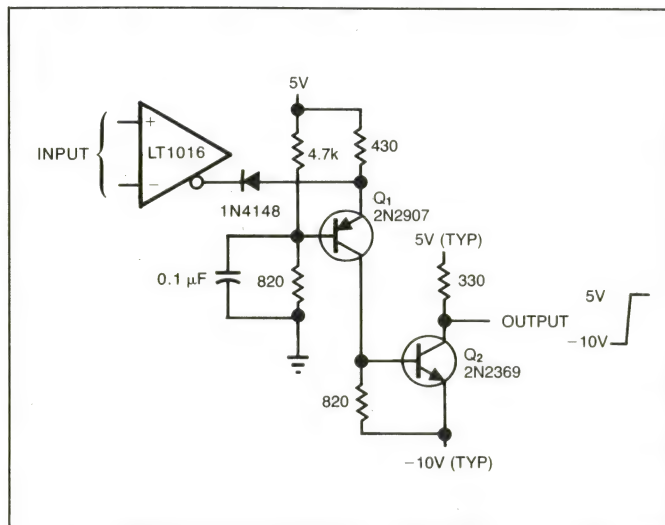


Fig 5—By adding two components, you can make this level shifter switch in only 3 to 4 nsec.

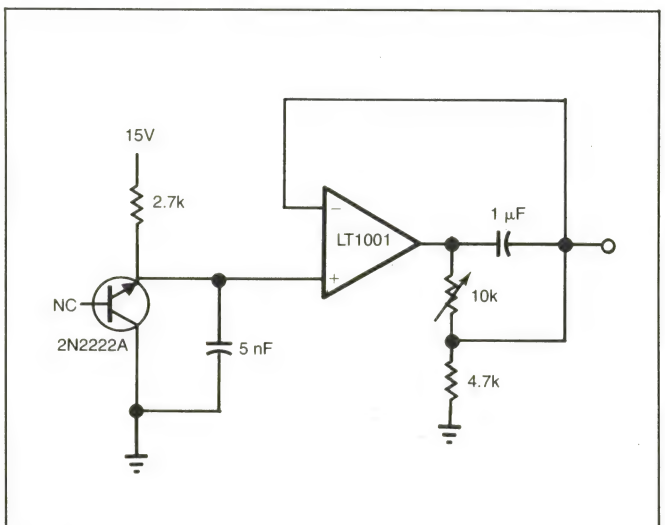


Fig 7—A mischievous gremlin lurks in this simple voltage-reference configuration. Find the gremlin and eliminate it.

In linear-circuit design, adding a few components often makes the difference between smooth performance and erratic, unpredictable operation.

suggests an application other than high-frequency amplification. Using only the user-accessible pins, sketch the application circuit. (Hint: You may ground the V+, V-, and output lines.)

9. Once you've determined the potential alternate use for the 733 in question 8, discuss the reasons why the reconfigured circuit might not work well.

10. Fig 9 shows a transistor that has suffered emitter-base breakdown. Predict the voltage at the collector and describe the mechanism that's responsible for the existence of this voltage level.

11. The 1.5V-powered A/D converter in Fig 10 is designed to operate over 25 to 35°C. The dual-transistor current source produces a ramp, which IC₁ com-

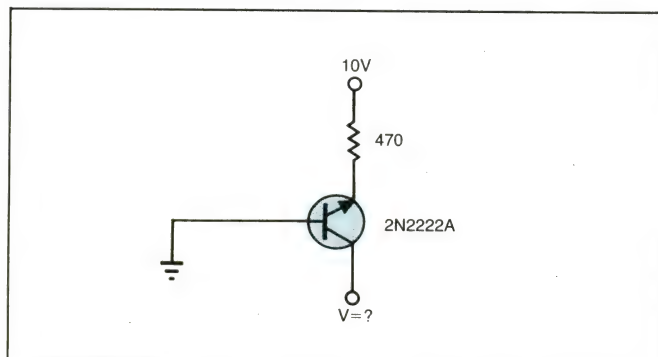


Fig 9—Test your knowledge of transistor trivia. Under the condition of base-emitter breakdown, what's the collector voltage in this circuit configuration?

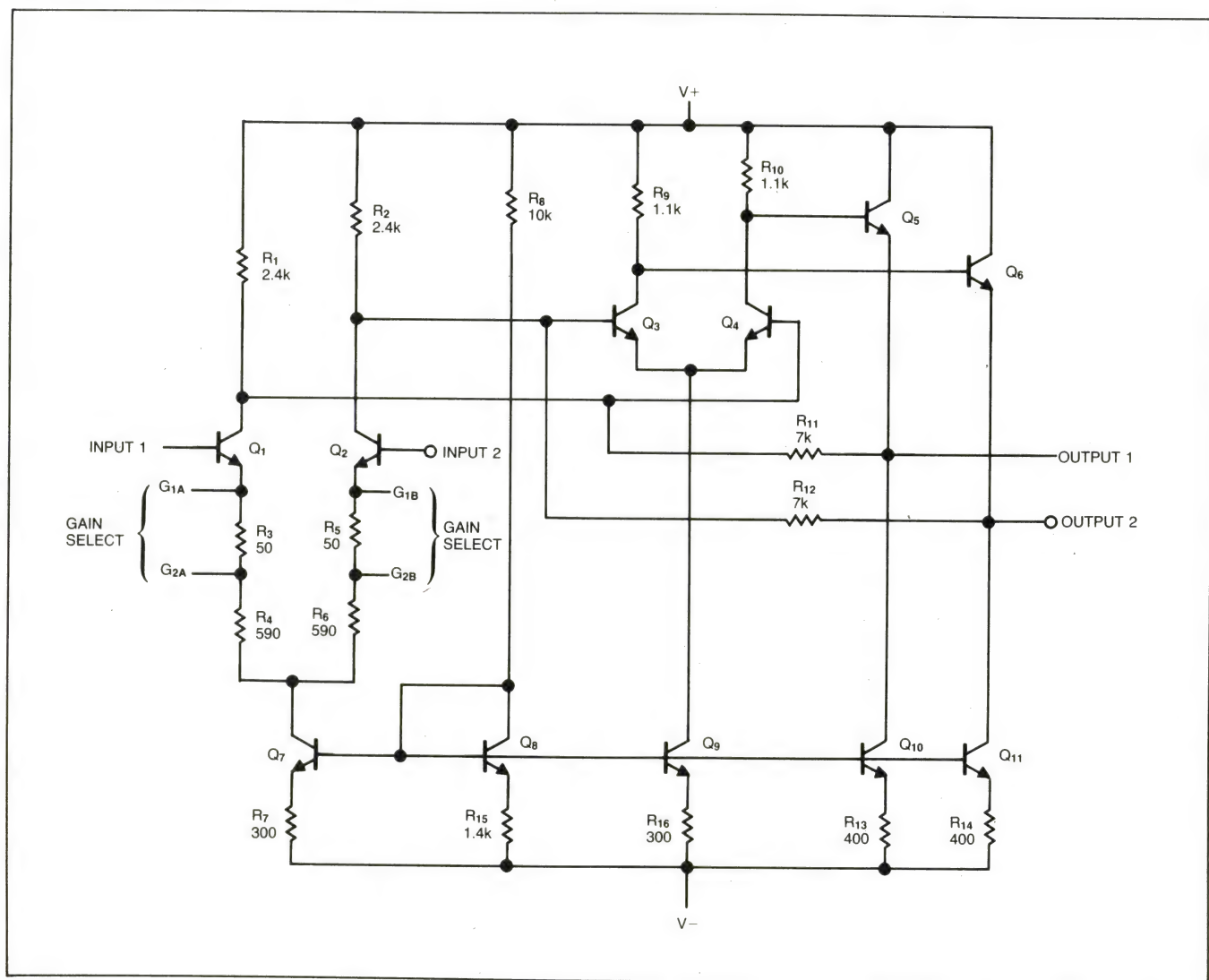


Fig 8—Find an unorthodox application for this monolithic video amplifier. You may ground any pins you like.

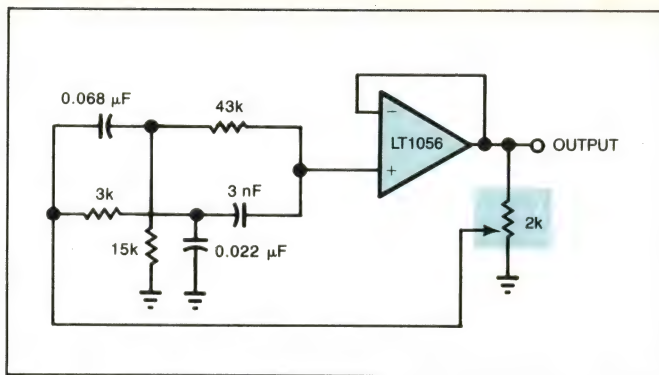


Fig 12—Predict the output of this unity-gain voltage follower, and discuss the role of the potentiometer.

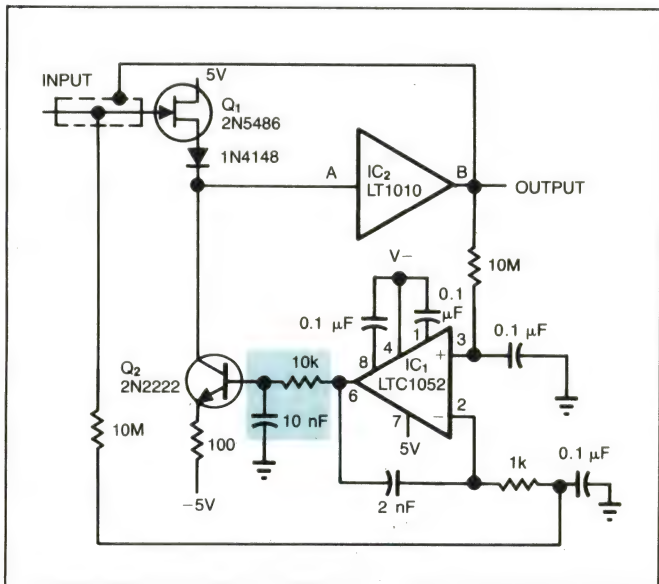


Fig 13—What's the role of the RC network in this fast, dc-stabilized FET buffer?

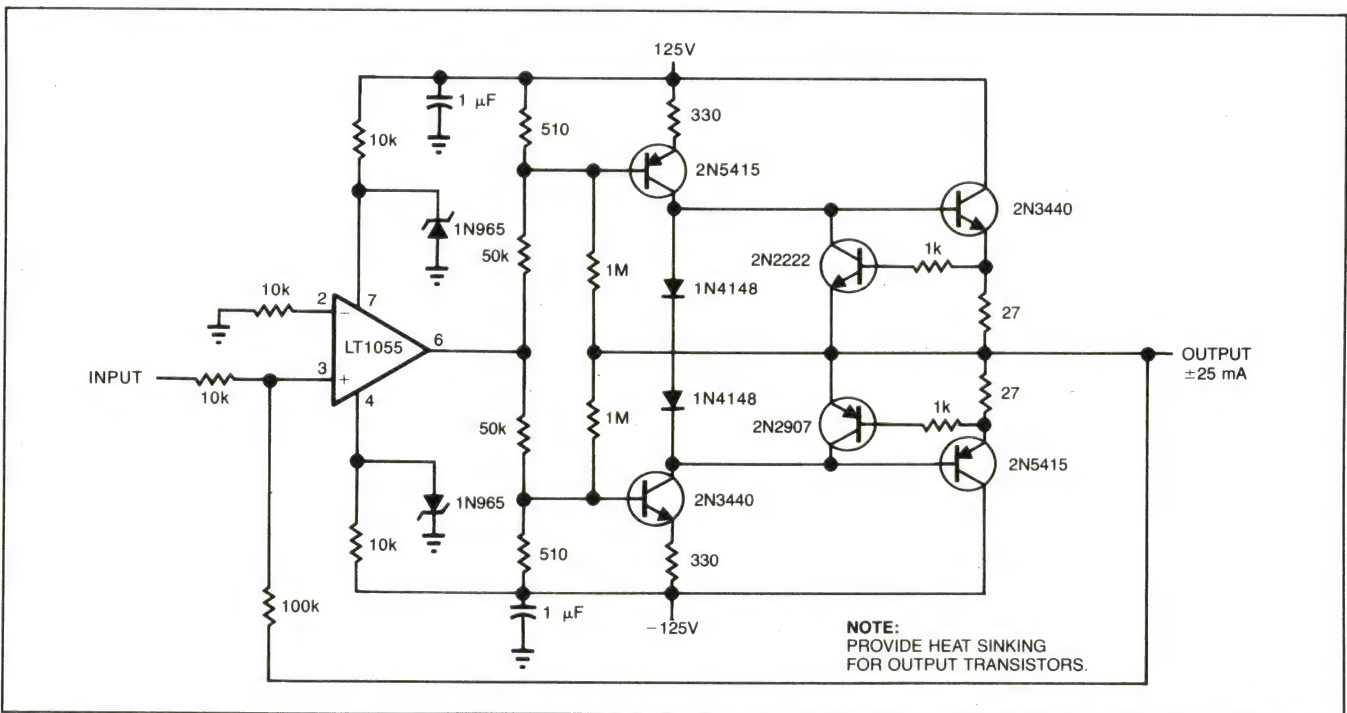


Fig 14—Add compensation to this 240V p-p, FET-input operational amplifier. What are the limitations on the circuit's high-frequency response?

compares with the input voltage. IC₁'s output status and the convert command gate IC₂'s output pulses to the output. The circuit takes 16 msec to perform a full-scale conversion and draws 360 μ A. It also has a large gain drift. Find the main source of this drift and correct it.

12. The broken lines in Fig 11 enclose a crude V/F converter that operates over a 1-Hz to 30-MHz range. Although this simple circuit is fast, its linearity is poor and drift exceeds 5000 ppm/°C. The remaining components form a quartz-locked, sampled-data loop that corrects the deficiencies. The loop works by counting the number of pulses at the LT1016's output during a fixed interval and by then converting this pulse count to a voltage (with the aid of the D/A converter). This voltage is compared with the circuit's input voltage by an amplifier that drives the LT1016 V/F converter.

This closed-loop technique relies on the stability of the time interval and the digital-to-voltage conversion to achieve circuit stability. Frequent updating of the loop ensures long-term stability. What are the frequency-resolution limitations of this circuit, and why do they compromise resolution? What governs the smallest possible input-related frequency change increment?

13. The circuit in Fig 12 is a unity-gain follower connected to a network of resistors and capacitors.

Stable dc characteristics and extended high-frequency performance aren't necessarily mutually exclusive. Clever stabilization tricks let you obtain both.

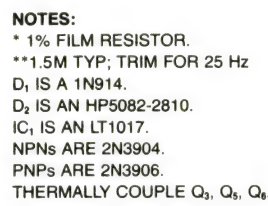


Fig 15—What's the approximate gain drift in this V/F-converter circuit, and what are the primary contributors to the drift figure?

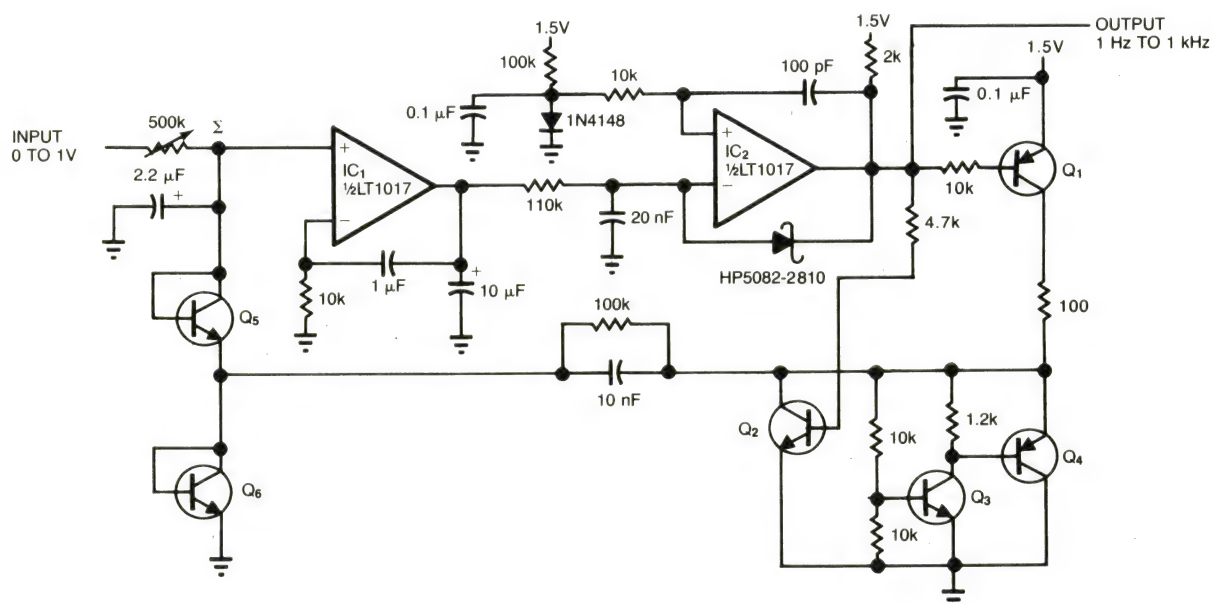


Fig 16—What's the secret of this 1.5V-powered V/F converter's low current consumption, and what tradeoffs do you have to make to achieve such low consumption?

It takes imagination and creativity to design linear circuitry that exploits the high speed and precision of modern linear ICs.

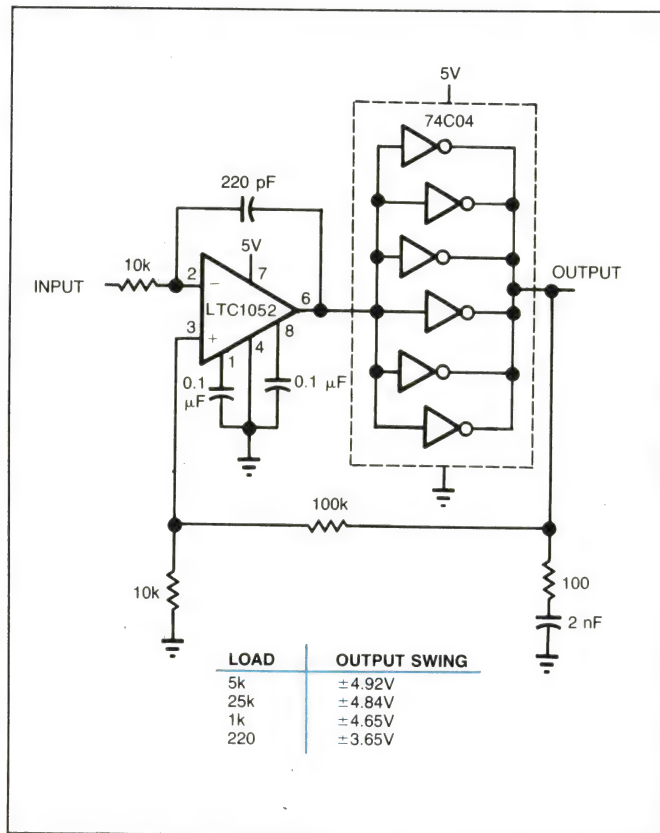


Fig 17—What are the power-supply constraints in this CMOS-output, chopper-stabilized operational amplifier?

What would you expect to see at the amplifier's output? What does the 2-kΩ potentiometer do?

14. Fig 13 shows a fast, dc-stabilized, low-capacitance FET buffer. The FET, configured as a source follower, drives the LT1010 buffer. The LTC1052 chopper-stabilized amplifier compares the dc voltages at the input and output of the LT1010, and it forces (via Q_2) the FET's channel current to control circuit offset. What is the function of the 10-kΩ/10-nF RC combination?

15. The circuit in Fig 14 has a $\pm 120\text{V}$ -swing output stage connected to an input stage that uses an LT1055 FET op amp. The LT1055 has a 5-MHz gain-bandwidth product. Frequency compensation for this circuit is not shown. Put it in. What limits this circuit's high-frequency response?

16. The 1.5V-powered charge-pump V/F converter in Fig 15 operates to 10 kHz. Which transistors must you thermally couple in order to obtain the best overall temperature coefficient in this circuit? Discuss the primary sources of gain drift in this configuration and estimate the gain temperature coefficient.

17. Fig 16 shows another 1.5V-powered V/F converter. This circuit provides a 1-kHz full-scale output. It draws only 125 μA of supply current—almost seven times less than does the circuit in Fig 15. What makes this reduction possible? What tradeoffs does the current reduction entail?

18. CMOS inverters serve as an output stage for the

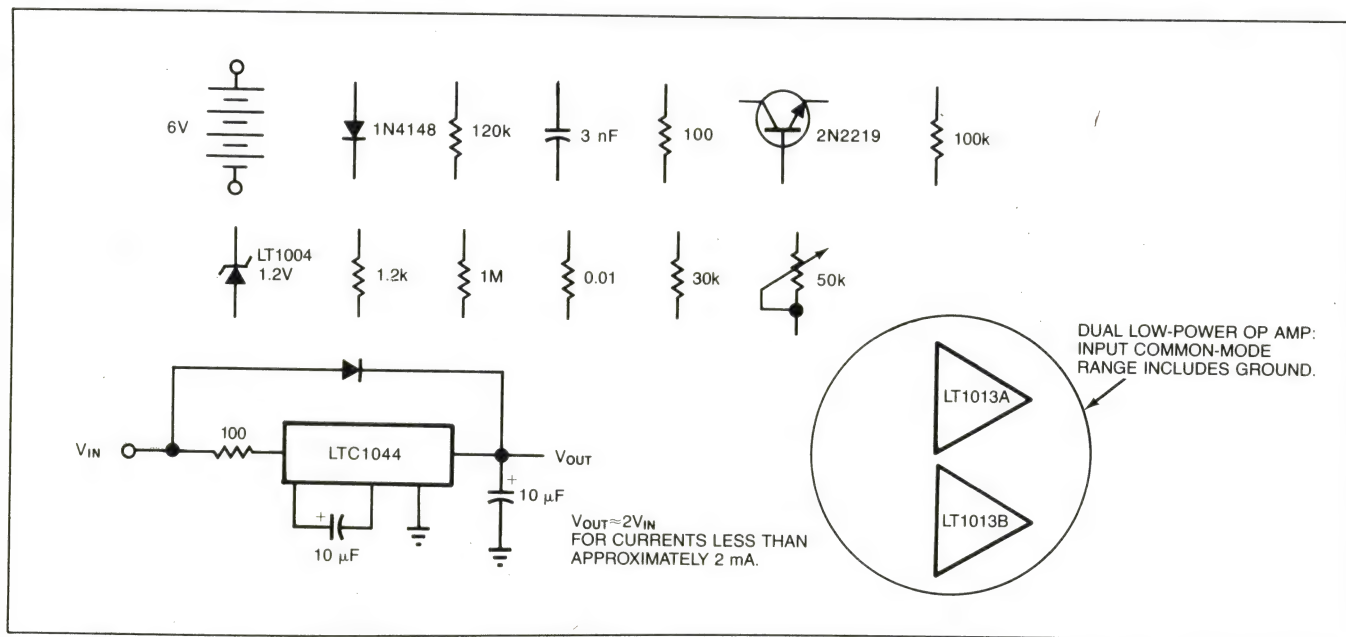
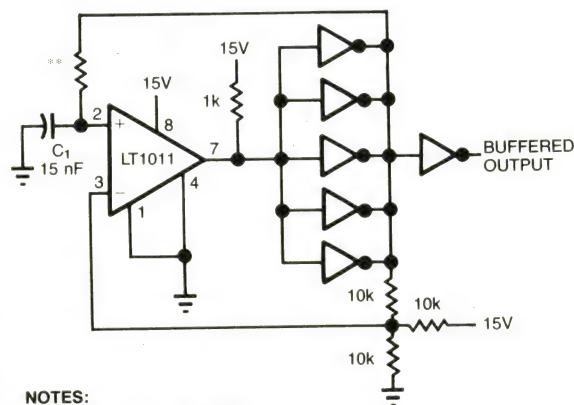


Fig 18—Use these building blocks to design a low-dropout, 5V regulator. Be sure to include short-circuit current limiting.

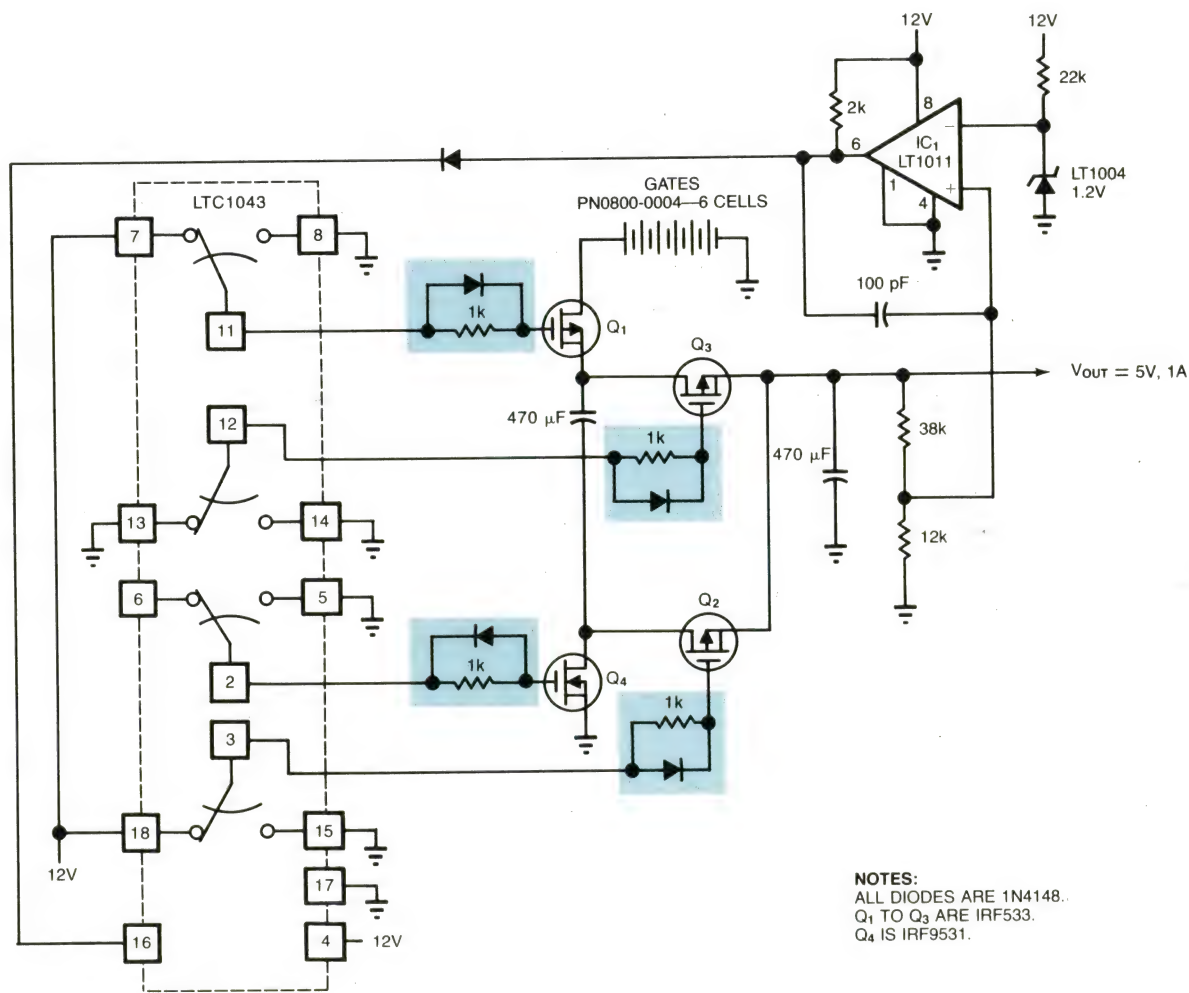
LTC1052 chopper-stabilized op amp in Fig 17. The damper network prevents oscillation, and the circuit works well as shown. Discuss power-supply restrictions—what supply voltages can you use in this circuit, and what voltages must you not use? Why?

19. Almost all low-dropout voltage regulators use pnp pass transistors. PNP-based designs provide low dropout, but they often have poor dynamic performance and relatively high quiescent currents. Using the components shown in Fig 18, construct a low-dropout, 5V regulator that operates from the 6V battery and provides 100-mA output. Include short-circuit limiting.



NOTES:
 **TRW MTR-5/+120 PPM/°C.
 25k ≤ R_S ≤ 200k
 C₁ IS WESCO 32-P POLYSTYRENE; -120 ± 30 PPM/°C.
 INVERTERS ARE 74HC04.

Fig 20—Analyze this RC oscillator. Discuss the role of the CMOS inverters, the influence of comparator characteristics, the temperature-drift performance, and the influence of operating frequency on drift.



NOTES:
 ALL DIODES ARE 1N4148.
 Q₁ TO Q₃ ARE IRF533.
 Q₄ IS IRF9531.

Fig 19—Discuss the roles of the diode-resistor networks in this switched-capacitor voltage inverter. Why are the networks present, and how do they function?

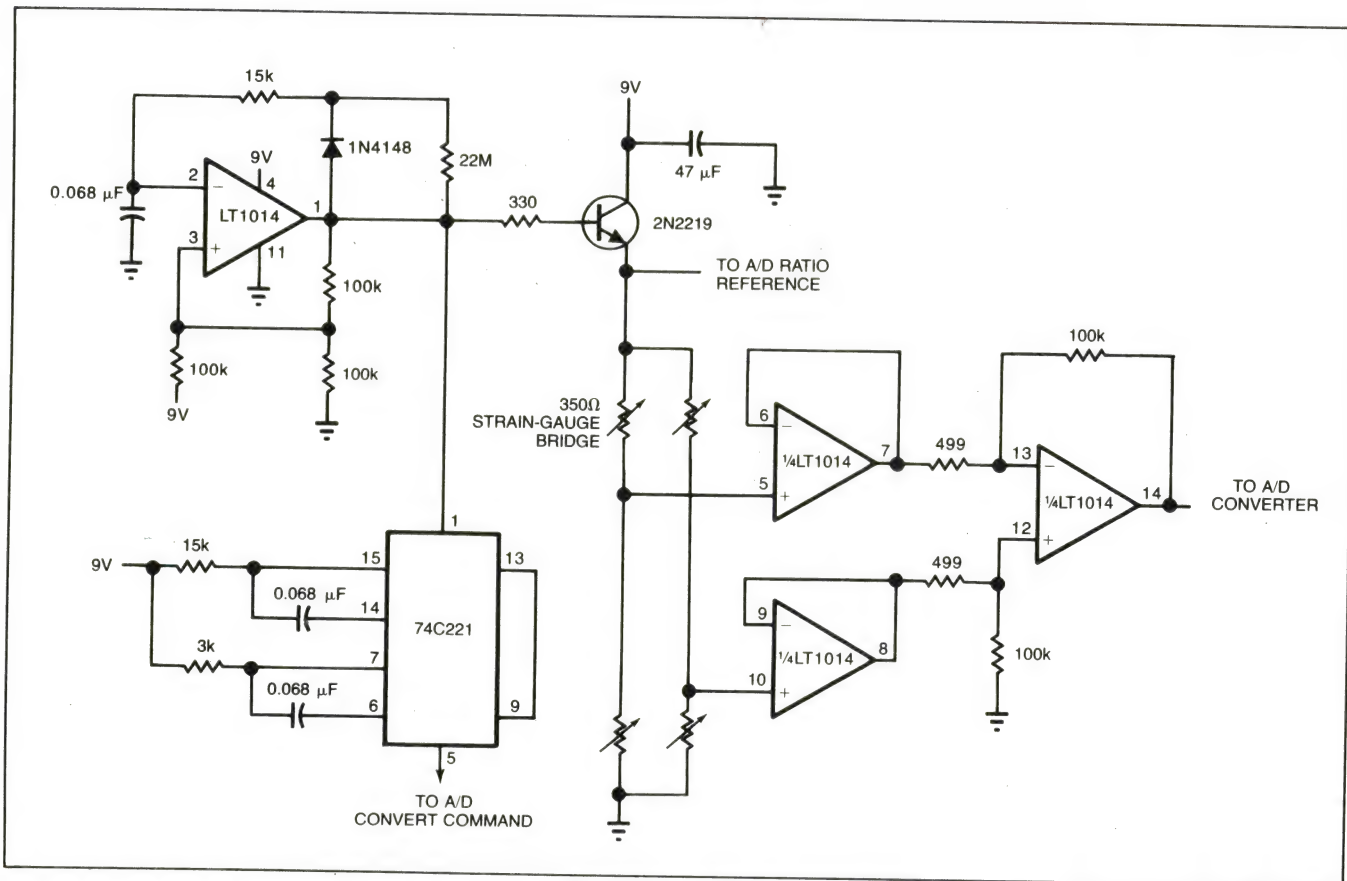


Fig 21—Can you find the subtle gremlin that degrades long-term accuracy in this sampled-operation strain-gauge signal conditioner?

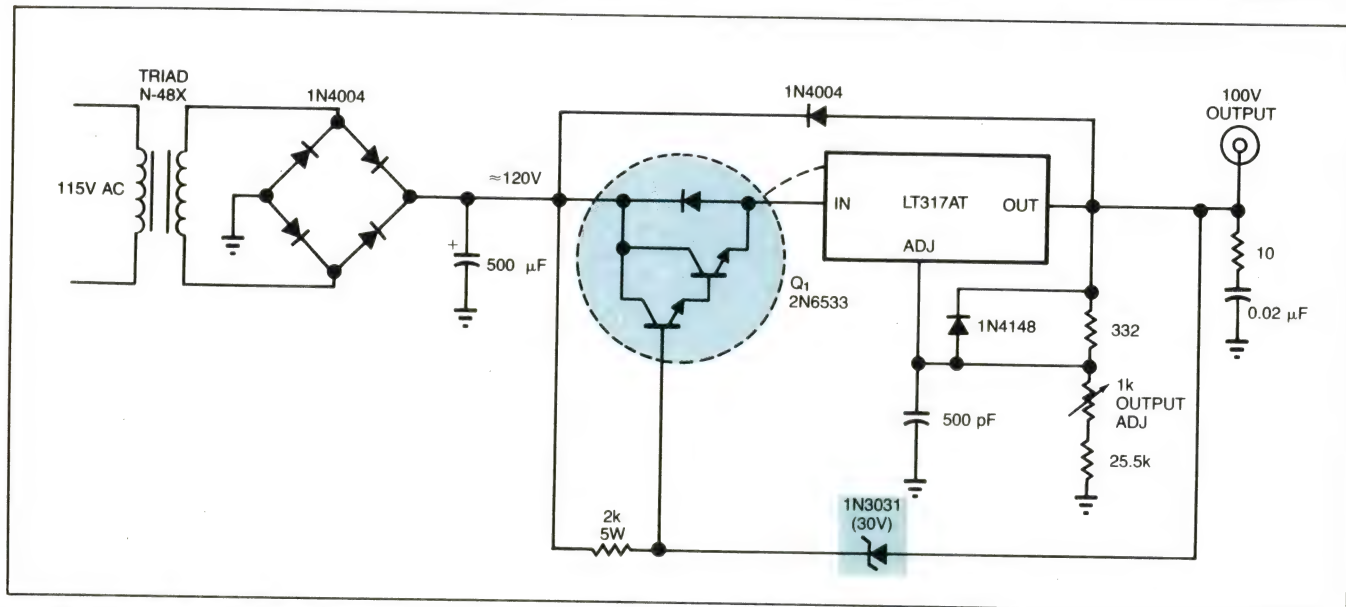
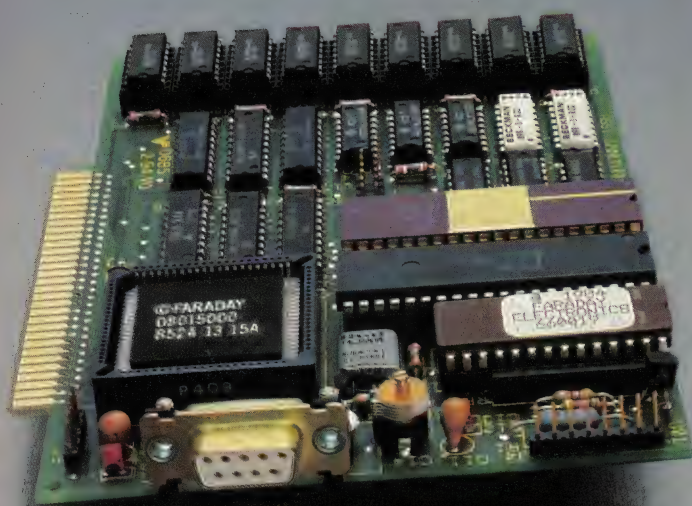


Fig 22—Discuss the roles of the transistor and the zener diode in this high-voltage regulator. What characteristics must Q_1 have, and how does the transformer type you choose influence your selection of Q_1 ?

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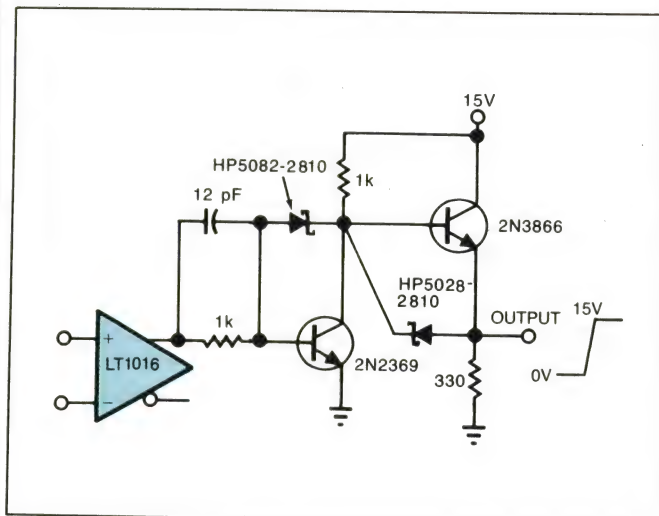


Fig 24—Halve the delay time in the level-shifting circuit at the output of the LT1016 TTL-output comparator.

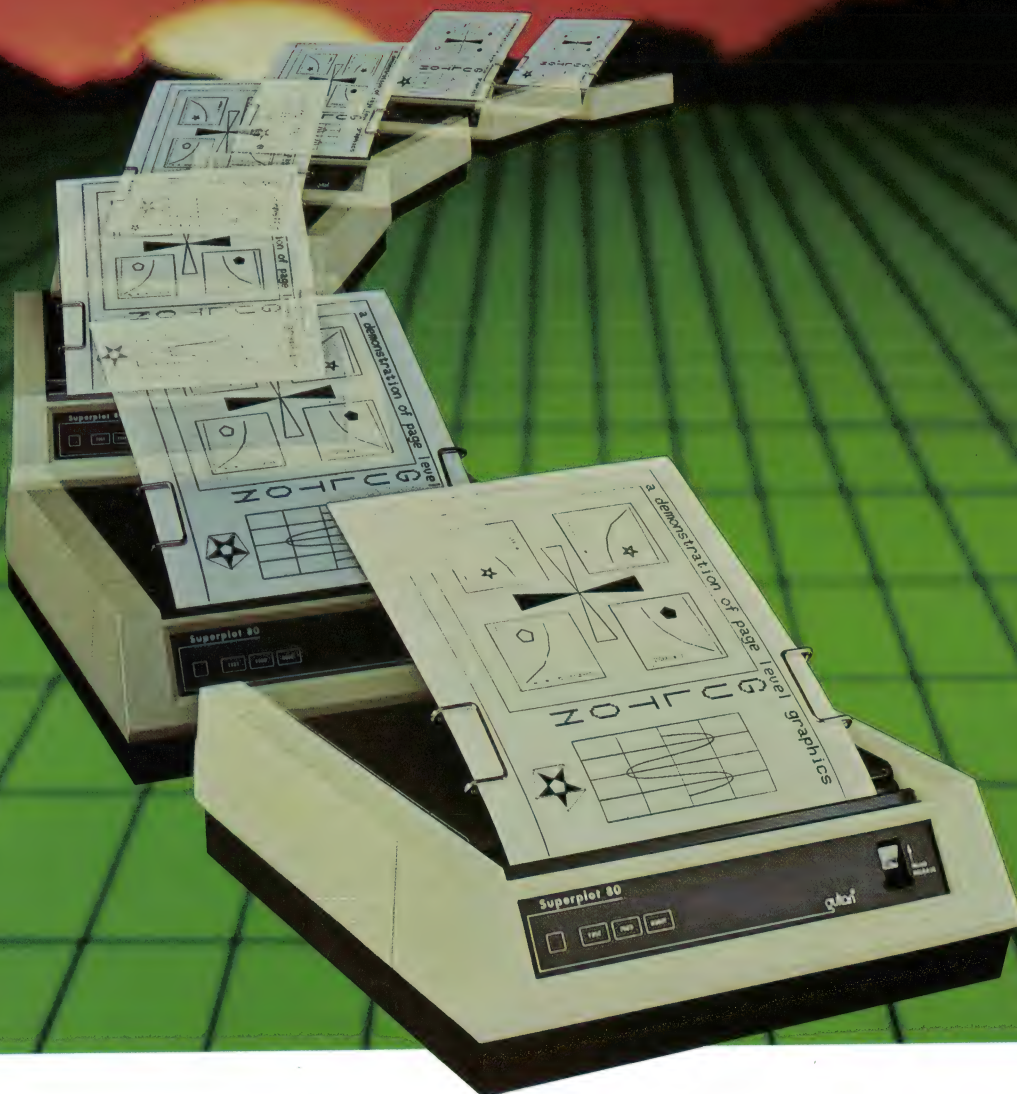
the noninverting input to null the offset. The LM669 has a maximum error of 25 μ V. What is the LTC1052 chopper-stabilized amplifier doing in the circuit? How could you simplify the circuit? How might you obtain power savings?

25. Fig 24 shows a level shifter for a fast TTL-output comparator. The level shifter's delay is approximately 8 nsec. Show a simple way to cut this delay in half.

Score yourself

After you've answered the 25 questions, compare your responses with the ones presented on page 155. Note that, as in Part 1, the answers to Part 2 are sometimes incomplete, and they sometimes pose additional questions for your reflection. Finally, be sure to circle the appropriate number in the Article Interest Quotient. Your response will count heavily in the author's decision to work on another analog-IQ quiz, or to give in and study ones and zeros (heaven forbid!). **EDN**

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


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Terence J Andrews, Consultant

Currently available error-detection and -correction (EDAC) chips cannot function fast enough to keep up with some high-speed memories. Fortunately, you need

not rely on commercial EDAC ICs; if you can tolerate a limitation to 8-bit-wide memories, you can design your own high-speed, PROM-based EDAC circuit. The PROM-based circuit generates check bits in 45 nsec and requires no clock or other control signals.

EDAC circuits correct common, intermittent failures of dynamic RAMs; these RAMs will occasionally change a bit or two in a stored word. EDAC memories—that is, memories equipped with EDAC circuitry—can correct single-bit errors in a word as that word is read from memory (see **box**, “EDAC: The conventional approach”). In addition, although they cannot correct double-bit errors, they can signal the computer if two bits in a given word are incorrect. Of course, there's a limit to the power of EDAC circuits; they will attempt to correct the wrong bits when three or more bits are in error. On the other hand, an EDAC unit can correct

TABLE 1—EDAC IC SPECIFICATIONS

MANUFACTURER	PART NUMBER	CHECK-BIT-GENERATING TIME	EDAC TIME	NUMBER OF BITS
TEXAS INSTRUMENTS, NATIONAL SEMICONDUCTOR	74ALS632	60 nSEC	90 nSEC	32
FAIRCHILD	74F632	35 nSEC	60 nSEC	32*
ADVANCED MICRO DEVICES	Am2960	40 nSEC	50 nSEC	16
INTEL, WESTERN DIGITAL	8206	60 nSEC	65 nSEC	16
TEXAS INSTRUMENTS, NATIONAL SEMICONDUCTOR	DP8400	40 nSEC	75 nSEC	16
FUJITSU	MB1412A	40 nSEC	50 nSEC	8

* ESTIMATED: UNITS NOT IN PRODUCTION AS OF AUGUST 9, 1985.

EDAC circuits correct common, intermittent failures of dynamic RAMs; these RAMs will occasionally change a bit or two in a stored word.

errors even if the error occurs in the check word itself and not just in the data word.

The design presented in this article substitutes PROMs for the commercial ICs' check-word-generating and error-correcting logic. This design adds only the access time of the PROMs to an EDAC memory's read and write cycles—about 40 nsec—and it's faster than commercial EDAC ICs (Table 1).

A glance at Table 2 shows that 16-bit-wide (or larger) memories would exceed the capacity of presently available PROMs. For example, an EDAC PROM for a

16-bit-wide memory would need 22 address lines and 4M bit locations.

TABLE 2—MEMORY REQUIREMENTS

DATA BITS	CHECK BITS	TOTAL BITS
8	5	13
16	6	22
32	7	39
64	8	72

In spite of the limitation to 8-bit-wide memories, you

LISTING 1—EDAC CALCULATION PROGRAM

```

100 PRINT "ENTER DATA BITS (D0 THRU D7) TO BE WRITTEN TO MEMORY"
110 PRINT "SEPARATE THE EIGHT BITS WITH COMMAS"
120 INPUT D0%,D1%,D2%,D3%,D4%,D5%,D6%,D7%
130 C0%=D1% XOR D2% XOR D3% XOR D5%
140 C1%=D0% XOR D1% XOR D2% XOR D4% XOR D6%
150 C2%=D0% XOR D3% XOR D4% XOR D7% XOR 1%
160 C3%=D0% XOR D1% XOR D5% XOR D6% XOR D7% XOR 1%
170 C4%=D2% XOR D3% XOR D4% XOR D5% XOR D6% XOR D7%
180 PRINT "DATA BITS WRITTEN TO MEMORY"
190 PRINT "D0 D1 D2 D3 D4 D5 D6 D7"
200 PRINT D0%;D1%;D2%;D3%;D4%;D5%;D6%;D7%
210 PRINT "CHECK BITS WRITTEN TO MEMORY"
220 PRINT "C0 C1 C2 C3 C4"
230 PRINT C0%;C1%;C2%;C3%;C4%
240 PRINT "ENTER DATA BITS (D0 THRU D7) TO READ FROM MEMORY"
250 PRINT "SEPARATE THE EIGHT BITS WITH COMMAS"
260 INPUT E0%,E1%,E2%,E3%,E4%,E5%,E6%,E7%
270 PRINT "ENTER CHECK BITS (C0 THRU C4) TO BE READ FROM MEMORY"
280 PRINT "SEPARATE THE FIVE BITS WITH COMMAS"
290 INPUT F0%,F1%,F2%,F3%,F4%
300 PRINT "DATA BITS READ FROM MEMORY"
310 PRINT "D0 D1 D2 D3 D4 D5 D6 D7"
320 PRINT E0%;E1%;E2%;E3%;E4%;E5%;E6%;E7%
330 PRINT "CHECK BITS READ FROM MEMORY"
340 PRINT "C0 C1 C2 C3 C4"
350 PRINT F0%;F1%;F2%;F3%;F4%
360 REM "GENERATE NEW CHECK BITS FROM DATA READ FROM MEMORY"
370 N0%=E1% XOR E2% XOR E3% XOR E5%
380 N1%=E0% XOR E1% XOR E2% XOR E4% XOR E6%
390 N2%=E0% XOR E3% XOR E4% XOR E7% XOR 1%
400 N3%=E0% XOR E1% XOR E5% XOR E6% XOR E7% XOR 1%
410 N4%=E2% XOR E3% XOR E4% XOR E5% XOR E6% XOR E7%
420 PRINT "GENERATE NEW CHECK BITS FROM MEMORY DATA BITS"
430 PRINT "N0 N1 N2 N3 N4"
440 PRINT N0%;N1%;N2%;N3%;N4%
450 PRINT "NEW CHECK BITS EXOR'ED WITH MEMORY CHECK BITS"
460 PRINT "TO GENERATE THE SYNDROME BITS"
470 Y0%=F0% XOR N0%
480 Y1%=F1% XOR N1%
490 Y2%=F2% XOR N2%
500 Y3%=F3% XOR N3%
510 Y4%=F4% XOR N4%
520 PRINT "Y0 Y1 Y2 Y3 Y4 ARE THE SYNDROME BITS"
530 PRINT Y0%;Y1%;Y2%;Y3%;Y4%
540 J%=Y0%+Y1%+Y2%+Y3%+Y4%
550 IF J%=0 THEN GOTO 630
560 REM "GET PARITY OF THE SYNDROME BITS"
570 Z%=Y0% XOR Y1% XOR Y2% XOR Y3% XOR Y4%
580 IF Z%=0 THEN PRINT "SYNDROME BIT PARITY IS EVEN"
590 IF Z%=1 THEN PRINT "SYNDROME BIT PARITY IS ODD"
600 IF Z%=1 THEN GOTO 650
610 PRINT "MORE THAN ONE BIT ERROR"
620 GOTO FINISH
630 PRINT "NO BIT ERRORS DETECTED"
640 GOTO FINISH

650 PRINT "ONE BIT ERROR --- INVERT BIT ";
660 REM "DECODE THE SYNDROME BITS"
670 K%=(1*Y1%)+(2*Y2%)+(4*Y3%)+(8*Y4%)
680 IF K%<>0 THEN GOTO 710
690 IF Y0%=0 THEN GOTO 710
700 PRINT "C0"\F0%=1% XOR F0%\GOTO CHECK
710 IF K%=1 THEN GOTO JC1
720 IF K%=2 THEN GOTO JC2
730 IF K%=4 THEN GOTO JC3
740 IF K%=5 THEN GOTO JD1
750 IF K%=7 THEN GOTO JD0
760 IF K%=8 THEN GOTO JC4
770 IF K%=9 THEN GOTO JD2
780 IF K%=10 THEN GOTO JD3
790 IF K%=11 THEN GOTO JD4
800 IF K%=12 THEN GOTO JD5
810 IF K%=13 THEN GOTO JD6
820 IF K%=14 THEN GOTO JD7
830 GOTO SMASH
840 CDATA:\PRINT "CORRECTED DATA BITS"
850 PRINT "R0 R1 R2 R3 R4 R5 R6 R7"
860 PRINT E0%;E1%;E2%;E3%;E4%;E5%;E6%;E7%
870 GOTO FINISH
880 CHECK:\PRINT "CORRECTED CHECK BITS"
890 PRINT "S0 S1 S2 S3 S4"
900 PRINT F0%;F1%;F2%;F3%;F4%
910 GOTO FINISH
920 JC0:\PRINT "C0"\F0%=1% XOR F0%
930 GOTO CHECK
940 JC1:\PRINT "C1"\F1%=1% XOR F1%
950 GOTO CHECK
960 JC2:\PRINT "C2"\F2%=1% XOR F2%
970 GOTO CHECK
980 JC3:\PRINT "C3"\F3%=1% XOR F3%
990 GOTO CHECK
1000 JC4:\PRINT "C4"\F4%=1% XOR F4%
1010 GOTO CHECK
1020 JD0:\PRINT "D0"\E0%=1% XOR E0%
1030 GOTO CDATA
1040 JD1:\PRINT "D1"\E1%=1% XOR E1%
1050 GOTO CDATA
1060 JD2:\PRINT "D2"\E2%=1% XOR E2%
1070 GOTO CDATA
1080 JD3:\PRINT "D3"\E3%=1% XOR E3%
1090 GOTO CDATA
1100 JD4:\PRINT "D4"\E4%=1% XOR E4%
1110 GOTO CDATA
1120 JD5:\PRINT "D5"\E5%=1% XOR E5%
1130 GOTO CDATA
1140 JD6:\PRINT "D6"\E6%=1% XOR E6%
1150 GOTO CDATA
1160 JD7:\PRINT "D7"\E7%=1% XOR E7%
1170 GOTO CDATA
1180 SMASH:\PRINT "???", "MULTIPLE ERROR?"
1190 FINISH:\END

```


EDAC: The conventional approach

The conventional way to provide error detection and correction (EDAC) is to employ one or more LSI chips designed expressly to perform 16- or 32-bit EDAC functions. **Fig A** shows a simplified block diagram of a typical EDAC unit and a memory array. (This EDAC example is generalized and does not resemble any particular manufacturer's product.)

The memory array consists of five check-bit RAMs and eight data-bit RAMs. The EDAC IC communicates with the memory array via the bidirectional data-bit and check-bit buses. The signals \overline{RAS} , \overline{CAS} , and \overline{WE} go to all 13 RAMs. The multiplexed address signals (MXA_0 to MXA_8) also go to all 13 RAMs.

During a write cycle, the eight data bits (D_0 to D_7) go to both the EDAC unit and the eight data-bit RAMs. Inside the EDAC circuit, the data bits go to the check-bit generator, which comprises five XOR gates. The check-bit generator produces five check bits (CB_0 to CB_4), which then go to the syndrome-bit generator.

RAM stores check bits

During a write cycle, the other inputs are forced to zero, so the check bits exit the syndrome-bit generator unchanged and are latched in the check-bit-output latch. The check bits then go to the five check-bit RAM chips via the check-bit bus.

During a read cycle, the data bits are read from memory onto the bidirectional data-bit bus and into the EDAC unit. From there they go once more to the check-bit generator to provide a new set of check bits, which then proceed to the syndrome-bit generator. In the meantime, the five previously stored check bits are read from memory and enter the EDAC circuit via the bidi-

rectional check-bit bus. These stored check bits are presented to the syndrome-bit generator. The five XOR gates of the syndrome-bit generator develop the five syndrome bits, Y_0 to Y_4 .

If the syndrome bits are all zero, then the stored check bits and the new check bits derived from the data memory's readout match and no errors have occurred. In any other case, an error has occurred, and the syndrome bits go to the bit-in-error (BIE) detection logic, which controls the correction logic.

Logic inverts error bit

The correction logic consists of eight 2-input XOR gates. One

input to each of these gates is a data bit read from memory. The BIE logic controls the other input. This logic inverts the data bit to be corrected using one of the XOR gates. The output of the correction logic latches into the data-output register, where it can be read onto the system's data bus.

The syndrome bits also go to the error-detect logic, which decodes the five bits to describe three possible conditions: no error, a single-bit error, and a double-bit error (see **Table 3** on pg 144). The error-detection logic provides the single-bit error or double-bit error signals for external error-handling logic.

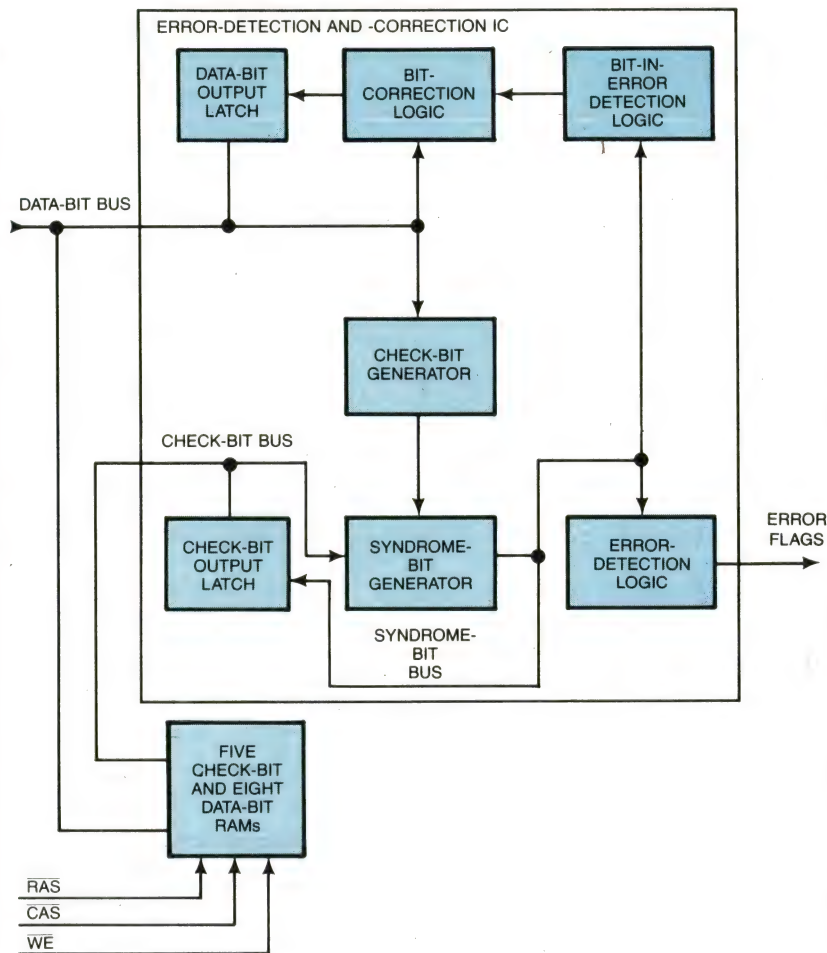


Fig A—Conventional EDAC ICs employ combinational logic and latches when performing the EDAC function.

Commercial EDAC ICs use combinational logic to derive a check word from each word stored into the memory.

can achieve memories of any bit width by paralleling 8-bit EDAC memory banks.

Fig 1's block diagram shows the 8-bit PROM-based EDAC-memory circuit. The eight data lines DI_0 to DI_7 go to both a $64k \times 8$ -bit data-bit RAM and to a 256×8 -bit check-bit-generating (CBG) PROM. The CBG PROM stores five check bits corresponding to every possible combination of input-data bits—256 in all. The CBG PROM's output is stored in a $64k \times 5$ -bit check-bit RAM. The data outputs of both RAMs (DO_0 to DO_7) go to the address lines of an $8k \times 15$ -bit EDAC PROM. This PROM, in turn, provides eight corrected data bits along with diagnostic and error-flag bits.

To understanding how this simple circuit operates, you should first note how it stores a data word. You access both the check-bit RAM and the data RAM, during a write cycle, with the same multiplexed row and column addresses and control signals: MXA_0 to MXA_8 , RAS , CAS , and WE . Consequently, the two memories effectively form a 13-bit-wide memory.

The data-bit RAM stores the data on data lines DI_0 to DI_7 . The same data goes to the address lines of the CBG PROM. The CBG PROM thus functions as a fast look-up table for check-bit values. The check-bit RAM stores the check bits that correspond to the input data.

During a read cycle, the output of the check-bit RAM and the data RAM go, in parallel, to the EDAC PROM bank. The EDAC PROM bank is, in effect, another look-up table, which contains the proper output for all possible correct and incorrect combinations of the eight data bits and five check bits. The output of the two

RAMs is a pointer into this table. Consequently, the EDAC PROMs provide eight correct data bits where possible (CD_0 to CD_7), five syndrome bits (Y_0 to Y_4), and two error flags (SBE and DBE), which denote single- and double-bit errors.

The syndrome bits aren't essential, but they prove useful for testing. Table 3 provides the decoding algorithm for interpreting the syndrome bits. Note that if all five bits are zero, no error has occurred. If the five bits generate odd parity, then a single-bit error has occurred. If the five bits generate even parity but are not all zeros, then an uncorrectable double-bit error has occurred.

TABLE 3—SYNDROME-BIT DECODING

Y_4	Y_3	Y_2	Y_1	Y_0	CORRECTION:
0	0	0	0	0	NONE
0	0	0	0	1	C_0
0	0	0	1	0	C_1
0	0	1	0	0	C_2
0	1	0	0	0	C_3
1	0	0	0	0	C_4
0	1	1	1	0	D_0
0	1	0	1	1	D_1
1	0	0	1	1	D_2
1	0	1	0	1	D_3
1	0	1	1	0	D_4
1	1	0	0	1	D_5
1	1	0	1	0	D_6
1	1	1	0	0	D_7

All possible addresses in the CBG and EDAC PROMs

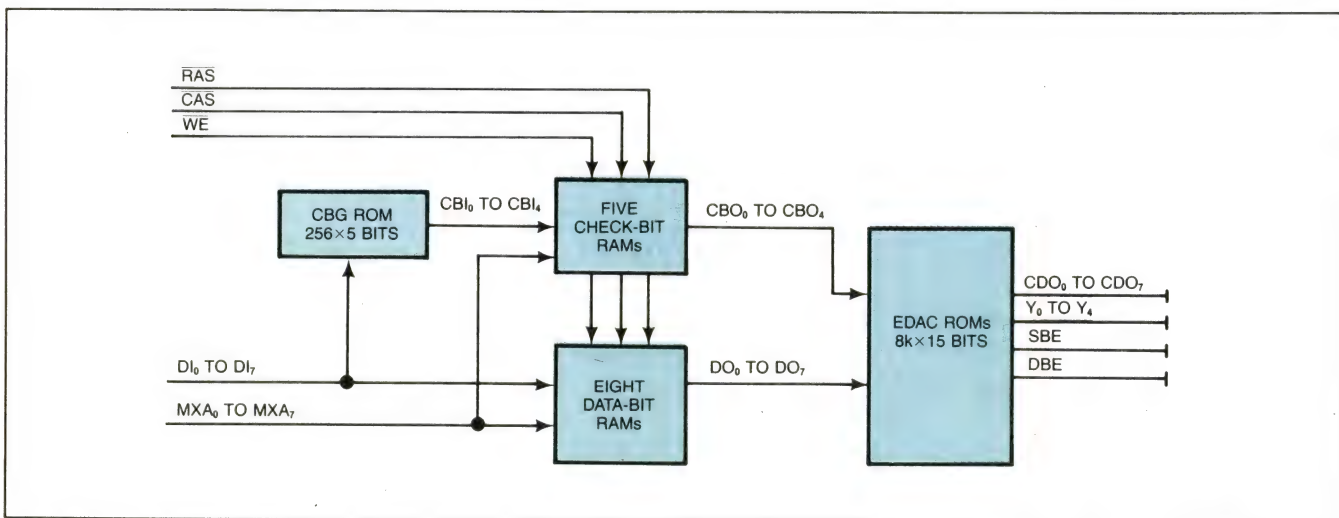


Fig 1—A PROM-based error-detection and -correction circuit adds only 40 nsec to an 8-bit-wide memory bank's access time. The EDAC circuit requires no clock or other control signals.

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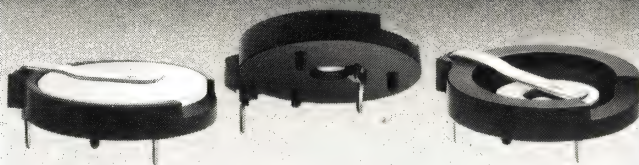
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are significant. The program in **Listing 1** on pg 142 generates the EDAC PROMs' code. The simple algorithm depicted in **Table 4** generates the check bits.

TABLE 4—CHECK-BIT ALGORITHM

	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	ONE
C ₀		•	•	•		•			
C ₁	•	•	•		•		•		
C ₂	•			•	•			•	•
C ₃	•	•				•	•	•	•
C ₄			•	•	•	•	•	•	

NOTE: XOR DOTTED DATA BITS TO GENERATE CORRESPONDING CHECK BIT.

Each dot in the table represents an input to an XOR function. For example, check bit C₀ is the XOR function of D₁, D₂, D₃, and D₅.

EDN

Author's biography

Terence J Andrews is an independent consultant working in the digital-design area. Terry attended the University of Nebraska at Omaha. In his spare time he enjoys electronics, astronomy, chess, and bowling.

Article Interest Quotient (Circle One)

High 479 Medium 480 Low 481

Answers to EDN's analog-IQ quiz Part 2

With the realization that the answers might be debatable, get ready to score Part 2 of your analog-design quiz. Each correct answer scores one point. After scoring, use the table below to determine your linear acumen.

1. Sampling of the motor's back EMF can't begin immediately after Q_3 turns off. When Q_3 turns off, the motor's inductive component produces a negative-going flyback voltage. The 1N4001 clamps this excursion at approximately $-1V$. If sampling were to occur at this point, the CD4016 would be subjected to this flyback-induced voltage, and ripple would result in the sampled output voltage. Q_2 , the $0.068\text{-}\mu F$ capacitor, and the 1N4148s address this problem. Grounded-base Q_2 turns on during the negative flyback interval, thus pulling the CD4016's control line to $0V$ (Q_2 's $V_{CE(SAT)}$ plus two 1N4148 drops approximate the 1N4001's forward drop), and preventing sampling.

SCORE YOURSELF

NUMBER OF QUESTIONS ANSWERED CORRECTLY	RATING
20 TO 25	DESIGNER OF REAL CIRCUITS
15 TO 19	DABBLER IN REAL CIRCUITS
10 TO 14	TTL/CMOS MANIPULATOR
5 TO 9	MICROPROCESSOR EXPLOITER
0 TO 4	SPEAKER OF COMPUTER TONGUES

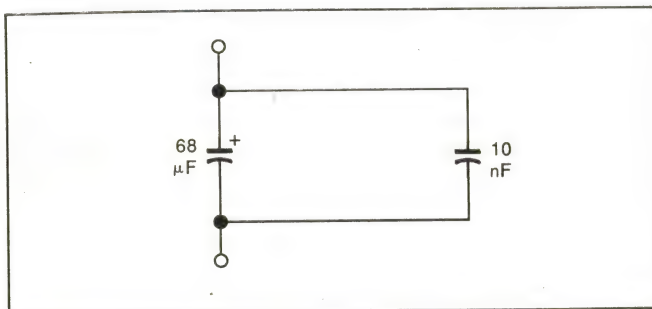


Fig 1—A simple parallel-capacitor network minimizes dc offsets while providing an ac ground over a wide frequency range.

When the clamped flyback voltage drops below Q_2 's V_{BE} , Q_2 turns off. The CD4016's control input ramps up at a rate set by the $0.068\text{-}\mu F$ capacitor's charge time. This charge time is such that the motor's negative flyback excursion has completely decayed by the time sampling commences. Thus, sampling occurs only during the back-EMF interval, and the sampled output is solely a function of back EMF.

2. Break the ground connection to the $1\text{-k}\Omega$ potentiometer and insert the network shown in **Fig 1**. This arrangement provides an ac ground over a wide frequency range, while eliminating dc-offset amplification.

3. The LM199-referenced, switched current sink can't function with the LM199 connected as drawn. To ensure that the voltage across the $3.5\text{-k}\Omega$ resistor tracks the LM199, connect the reference as shown in **Fig 2**.

4. Insert a tunnel diode between the $10\text{-k}\Omega$ -potentiometer/ 50Ω -resistor junction and ground.

5. To make the circuit switch in the 3- to 4-nsec range, add a feedforward capacitor (typically 1 nF)

Inductive flyback effects prevent accurate sampling of a motor's back EMF; you must install circuitry that inhibits sampling during the flyback interval.

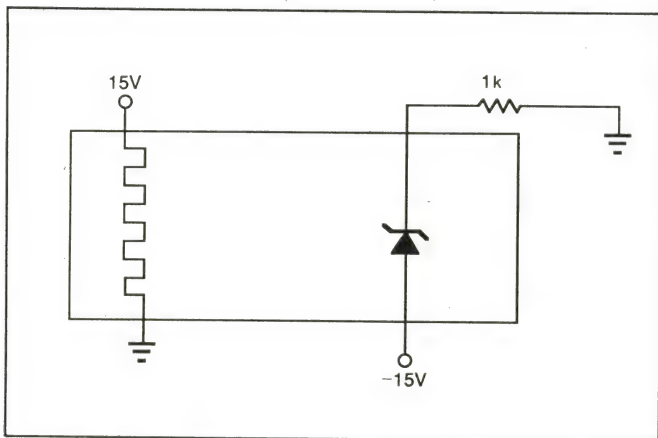


Fig 2—Corrected supply connections make the circuit in **Fig 3** on pg 128 function properly.

around the Q_1 stage. Connect it from the LT1016's inverting output to Q_2 's base. In addition, prevent Q_2 from saturating by using a Schottky diode to clamp the transistor's base-collector junction.

6. The crystal-oscillator circuit will operate reliably for crystal frequencies greater than 10 MHz if you insert an RC damper network from the LT1016's noninverting input to ground. (The resistor and capacitor should have values of approximately 22Ω and 820 pF.) Quartz crystals for frequencies approximately as high as 10 MHz are cut in such a way as to oscillate at their fundamental frequencies. At higher frequencies, the crystals operate in overtone mode, so they're likely to

oscillate at multiples of the desired frequency. The high gain-bandwidth product existing in the circuit as shown invites such undesirable operation. The damper network provides high-frequency attenuation; therefore, the crystal can't oscillate at a high-frequency overtone.

7. Beware! Transistors operating in the inverted mode often harbor a gremlin in the form of a negative-resistance characteristic. The oscilloscope photo in **Fig 3a** illustrates this phenomenon. This characteristic, with the aid of the 5-nF capacitor, produces a relaxation oscillator. The scope photo in **Fig 3b** shows the waveform at the transistor's emitter. The integrating capacitor in the LT1001's loop smooths the oscillations to an apparent dc level, but the output will seem noisy. Adding a 10-k Ω resistor before the 5-nF capacitor clears up the problem. Incidentally, pnp transistors don't exhibit this behavior. Why not?

8. By adding two resistors and an op amp (as shown in **Fig 4**), you can theoretically construct a thermal rms-to-dc converter around the 733's input stage. The input voltage produces heating in R_3 , thereby forcing Q_1 's V_{BE} to decline. This drop causes an imbalance in IC_1 's input voltages and causes the amplifier to drive R_5 . As R_5 heats up, it warms Q_2 , thus balancing IC_1 's input voltages. IC_1 's output voltage represents the rms (heating-energy) value of the input voltage, regardless of its frequency or wave shape.

9. Problems with using the 733 for the rms-to-dc function include mismatch between Q_1 and Q_2 , mismatch between R_3 and R_5 , and inappropriate thermal

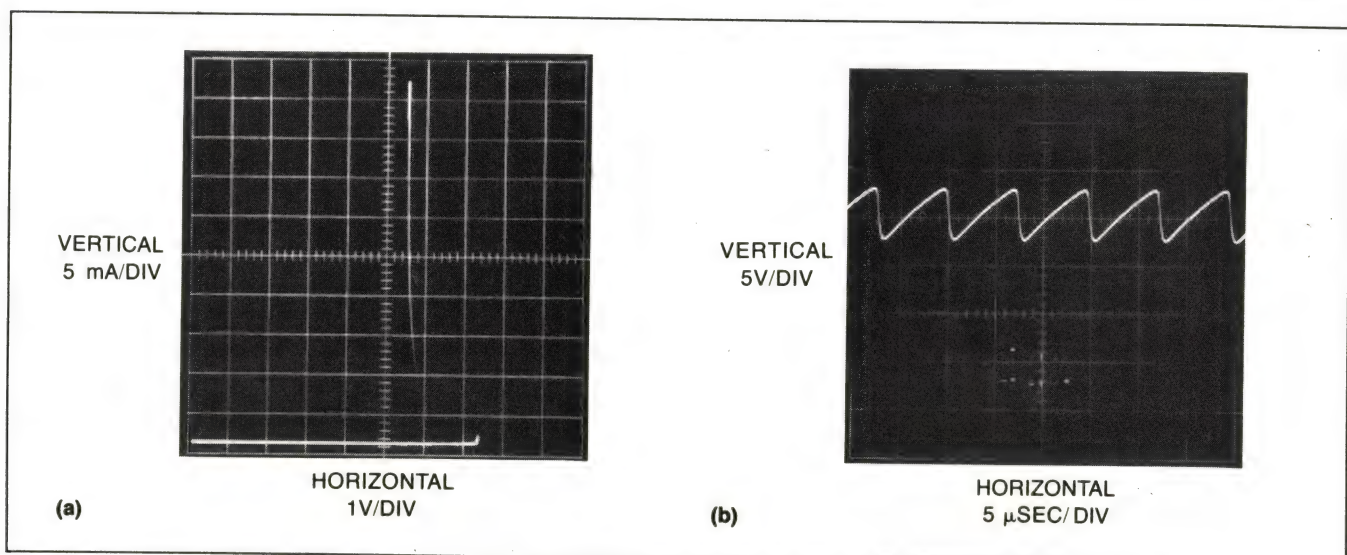


Fig 3—Negative resistance is an undesirable side effect that often arises when you operate transistors in the inverted mode (a). The phenomenon results in sawtooth oscillation (b).

layout of the 733 die. In particular, the thermal characteristics of the die might not be as symmetrical as the schematic diagram suggests. As a result, the single die promotes undesired thermal crosscoupling between the transistor and resistor pairs. You can, in fact, make the 733 function in this application, but it won't function very well.

10. The voltage at the collector measures 100 to 200 mV of *negative* polarity. The mechanism of operation is a photovoltaic one. The base-emitter junction, heated to incandescence, emits photons, causing photovoltaic activity at the collector.

11. If you connect a 1.2V supply to the circuit, the current source in the diagram will have an output that varies proportionally with absolute temperature. **Fig 5** shows a source that doesn't exhibit this problem.

12. Although it's not immediately obvious, this V/F converter's resolution is not restricted by the D/A converter's quantization limitations. The loop forces the converter's LSB to oscillate around the ideal value. The loop-compensation capacitor integrates this oscillating

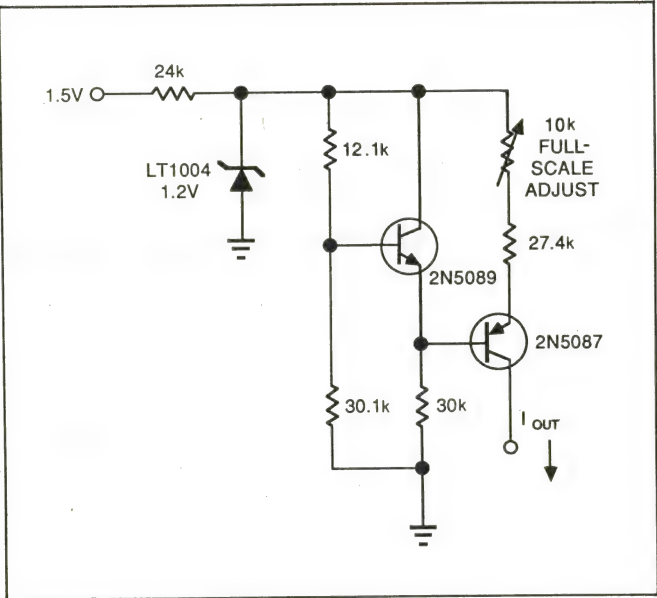


Fig 5—This temperature-drift eliminator circuit is a better current source than the one in **Fig 10** on pg 131.

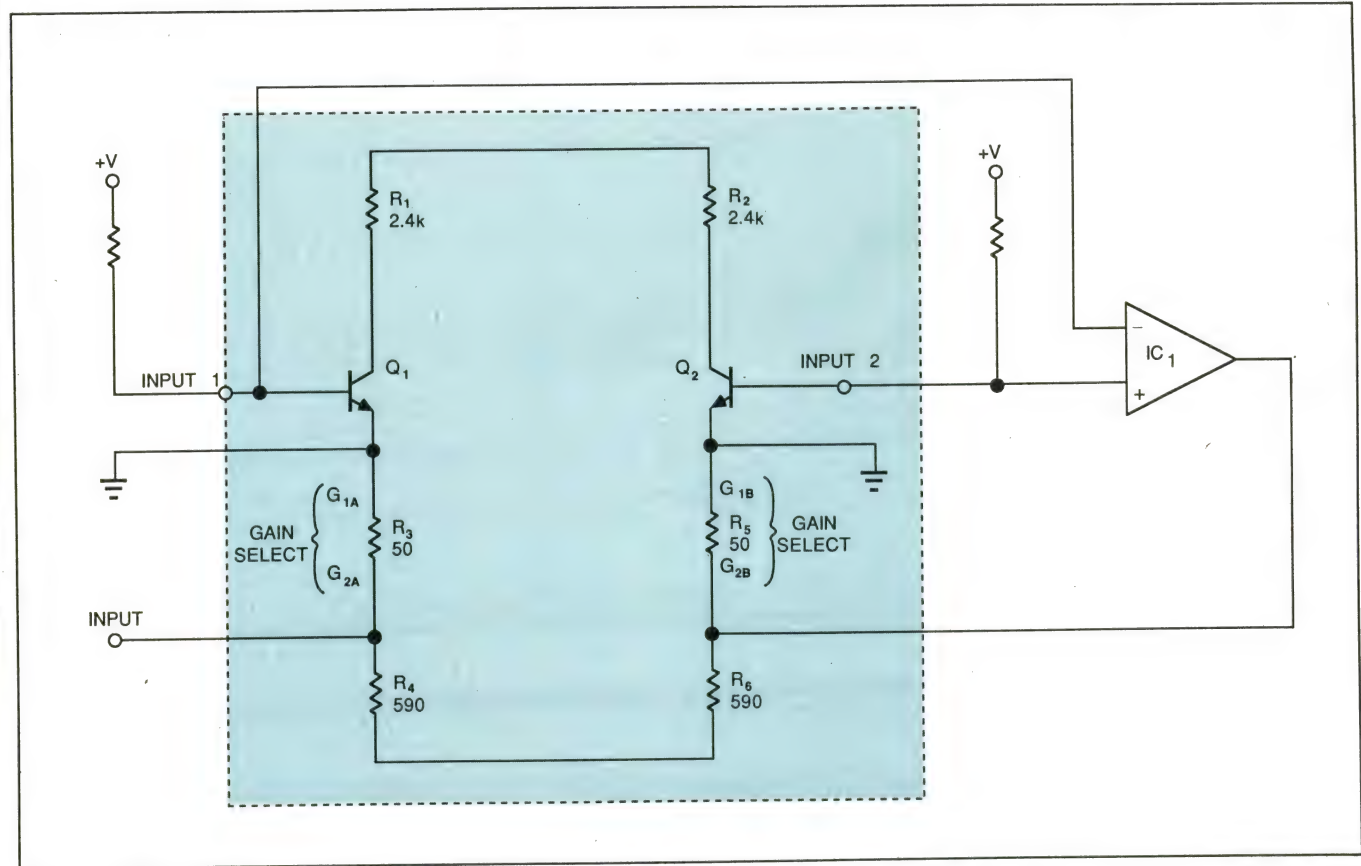


Fig 4—In an unorthodox application, the input stage of a $\mu A733$ video amplifier forms an rms-to-dc converter.

A simple capacitor can eliminate dc offset voltages while providing a good ac ground.

waveform to a dc level. Hence, the circuit tracks input shifts that are much smaller than the converter's LSB. Typically, a 12-bit (4096-step) D/A converter yields resolution of one part in 100,000. Circuit linearity, however, depends on the converter's linearity spec.

13. In theory, phase shift and gain are necessary to produce oscillation. Because the LT1056 operates at unity gain, it appears impossible for this circuit to oscillate, but oscillate it does. The amplifier's output is an 800-Hz waveform. The potentiometer adjusts the amount of feedback presented to the RC network. With too much feedback, the network doesn't oscillate; too little feedback produces saturation limiting. A proper feedback setting results in a reasonable sinusoidal output. But solve the real mystery: Where is the necessary gain hiding in the circuit?

14. The 10-k Ω /10-nF RC combination prevents IC₁'s output from experiencing high-speed, input-related signals that couple through Q₂'s collector-base junction capacitance. Without this RC network, IC₁'s output will necessarily contain high-frequency components that it can't servostabilize, and the stabilizing loop will be noisy.

15. Connect a local capacitor of approximately 100 pF from the output to the inverting input of the LT1055. This capacitor causes the amplifier's gain-bandwidth response to roll off before the signal reaches the output stage. A 30-pF global loop-compensation capacitor across the 100-k Ω feedback resistor will optimize overall response. The circuit's operating-frequency limitation is the high capacitance of the high-voltage transistors' junctions. The circuit's full-power response is typically 20 kHz.

16. Couple Q_3 , Q_5 , and Q_6 to obtain the best temperature compensation. The sources of gain drift include the 10-nF capacitor, the Q_3 - Q_4 reference, the Q_5 - Q_6 charge-steering transistors, and the input resistor. Q_5 and Q_6 substantially cancel Q_3 's V_{BE} -induced drift. The capacitor, a polystyrene type, has about 120-ppm/ $^{\circ}\text{C}$ drift; the input resistor has a drift of approximately 50 ppm/ $^{\circ}\text{C}$. The overall temperature coefficient from all sources should be in the 200- to 300-ppm/ $^{\circ}\text{C}$ range.

17. In the circuit shown, Q_1 is on most of the time, driving the Q_3 - Q_2 reference. Q_1 turns off only during the circuit's discharge cycle, which is approximately a 25- μ sec period set by the 100-pF/10-k Ω combination.

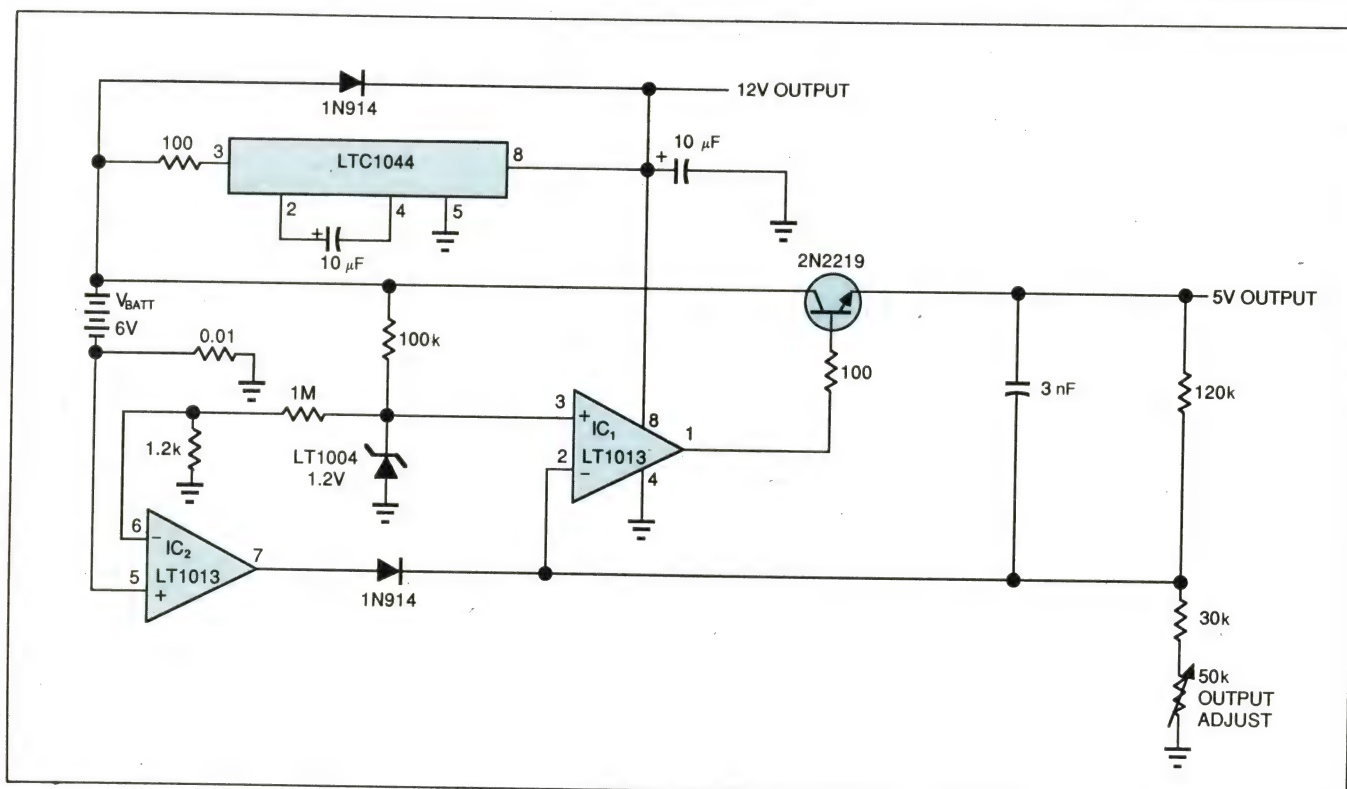


Fig 6—Configured as a voltage doubler in this circuit, the LTC1044 provides overdrive to the npn pass transistor, yielding low dropout voltages.

Even with output frequencies as high as 10 kHz, the best-case, on-time duty cycle is 50%. Thus, the power dissipated in the 330Ω resistor is

$$\frac{1}{2}[(1.5V - V_{CE(SAT)} - V_{REF}) \div 330\Omega],$$

where $V_{CE(SAT)}$ is the collector-emitter saturation voltage of Q_1 , or

$$\frac{1}{2}[(1.5V - 100\text{ mV} - 1V) \div 330\Omega] = 600\text{ }\mu\text{A}.$$

The circuit in Fig 16 on pg 133 uses a similar charge-pump feedback scheme, but IC_1 functions as a servo amplifier that controls the frequency of IC_2 , a free-running oscillator. This arrangement allows short Q_1 on-state times, thereby cutting power loss. The main tradeoff is the response time to input steps. The design in Fig 15 on pg 133 responds within one or two cycles of the new frequency. The Fig 16 circuit, however, must wait for the servo amplifier's loop poles to settle, which typically takes 100 msec.

18. The obvious power-supply restriction is the LTC1052's 18V limit. A less obvious constraint is that the 74C04 can operate as a power booster only in single-supply applications. Dual supplies would cause high idling current in the output stage, which, in turn, would cause excessive dissipation in the 74C04. The high dissipation would arise because both n- and p-channel devices conduct in a dual-supply application.

19. The most unusual feature of the design in Fig 6 is the use of the LTC1044 to provide voltage overdrive to the npn pass element's base. The 1044 provides this overdrive by doubling the battery's voltage and supplying this potential to the LT1013 control amplifier. Voltage overdrive to the npn emitter follower results in low dropout. If the circuit produces a 10-mA output, the dropout is only 15 mV. At 100-mA output, the dropout increases to 95 mV.

20. The diode/1-kΩ networks work with the high input capacitance of the MOSFETs to create turn-on and turn-off delays. Diode polarity determines whether a delay occurs on turn-on or turn-off. These delays prevent cross-conduction in the MOSFETs, thereby maximizing overall circuit efficiency and preventing the MOSFETs from being destroyed.

21. The circuit is a standard comparator-multivibrator configuration with parallel CMOS inverters between the comparator's output and the feedback resistors. In this scheme, the superior on-state characteristics of the MOS devices replace the relatively large and

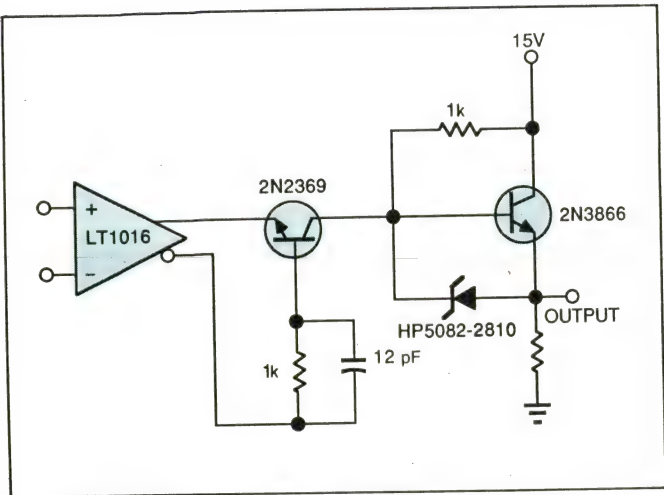


Fig 7—Reversing base and emitter voltages makes this circuit switch more rapidly than the circuit in Fig 24 on pg 138.

unstable V_{CE} -saturation losses of the comparator's bipolar output. Not only are the MOS switching losses to the rails low and resistive, but they tend to cancel out. The parallel connection of the inverters further reduces errors to insignificant levels. With this arrangement, the charge and discharge time constant of the capacitor is almost totally immune to supply and temperature shifts.

The 10-kΩ resistors need not be precision types, because, theoretically, resistor-value shifts will cancel out. In addition, the effect of the comparator's dc input errors is also negated, because of the symmetrical nature of the oscillator. Thus, the RC network is the only significant contributor of error. The nominal -120-ppm/°C temperature coefficient of the polystyrene capacitor is partially offset by the opposing temperature coefficient inherent in the specified resistor. In practice, you can obtain only a first-order compensation, because the capacitor's exact temperature coefficient is uncertain. A 0 to 70°C excursion typically has a 15-ppm/°C coefficient; the power-supply rejection factor is typically less than 200 ppm/V. Because of comparator propagation delays, circuits of this type are less stable at operating frequencies greater than 5 kHz.

22. To avoid possible long-term degradation of the transfer characteristic's accuracy, insert an RC filter between the oscillator's output and the 330Ω resistor that's connected to the 2N2219. For the RC filter, values of 4.7 kΩ and 10 nF produce satisfactory results. Without this network, the quickly rising steps applied to the strain bridge can have deleterious effects on the

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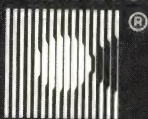
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bridge. For instance, a shift will develop slowly in the bonds between individual strain gauges and the mechanical beam. The filter eliminates the high dV/dt slope, thereby preventing the fast-rise problem. Incidentally, with the filter added, it's tempting to delete the 330Ω unit, but it's not a good idea. Why not?

23. The 30V zener diode prevents the voltage across the LT317A from rising to destructive levels under short-circuit conditions. When a short circuit occurs, the diode conducts, and Q_1 's emitter clamps at a level 2V lower than the zener voltage. Under these conditions, Q_1 's dissipation capability must be great enough to withstand the voltage across, and the current through, the transistor. One way to minimize the dissipation requirements for Q_1 is to select a transformer that can supply only a small amount of short-circuit current.

24. The LTC1052 amplifier corrects the $25\text{-}\mu\text{V}$ error in the LM669 by measuring the error at the LM669's input, comparing it with 0V, and then driving the LM669's reference input. The LTC1052's $5\text{-}\mu\text{V}$ offset-voltage specification improves the LM669's performance by a factor of 5.

To simplify the circuit, you could remove the connections from the LM669 to the $10\text{-k}\Omega/10\Omega$ divider. Further, drive the divider from the LTC1052's output (disconnect and remove the $500\text{-k}\Omega/50\Omega$ divider from the LTC1052's output). Finally, to save power, disconnect the LM669 from the power supply.

25. When the LT1016 in Fig 7's circuit switches, the 2N2369's base and emitter voltages reverse, causing the transistor to switch more rapidly than does the common-emitter stage in Fig 24 on pg 138. **EDN**

Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in related capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.



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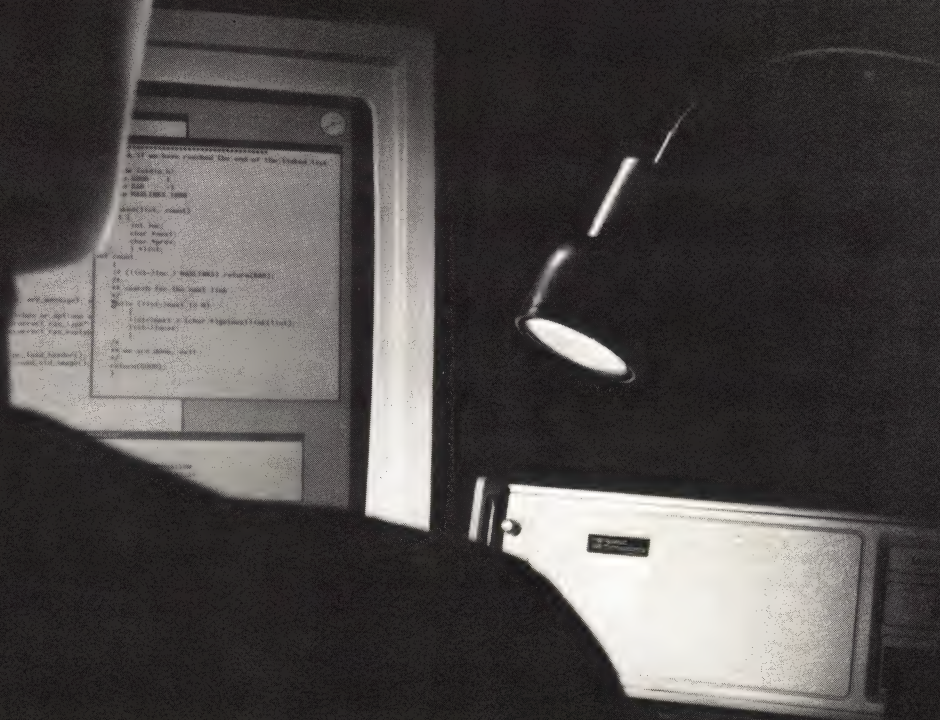
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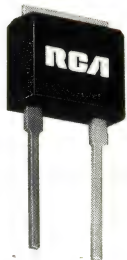
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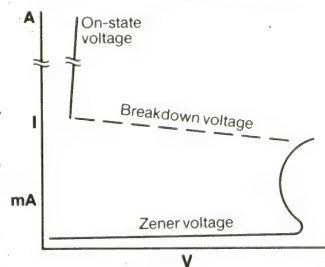
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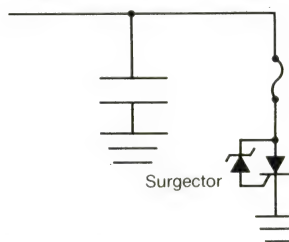
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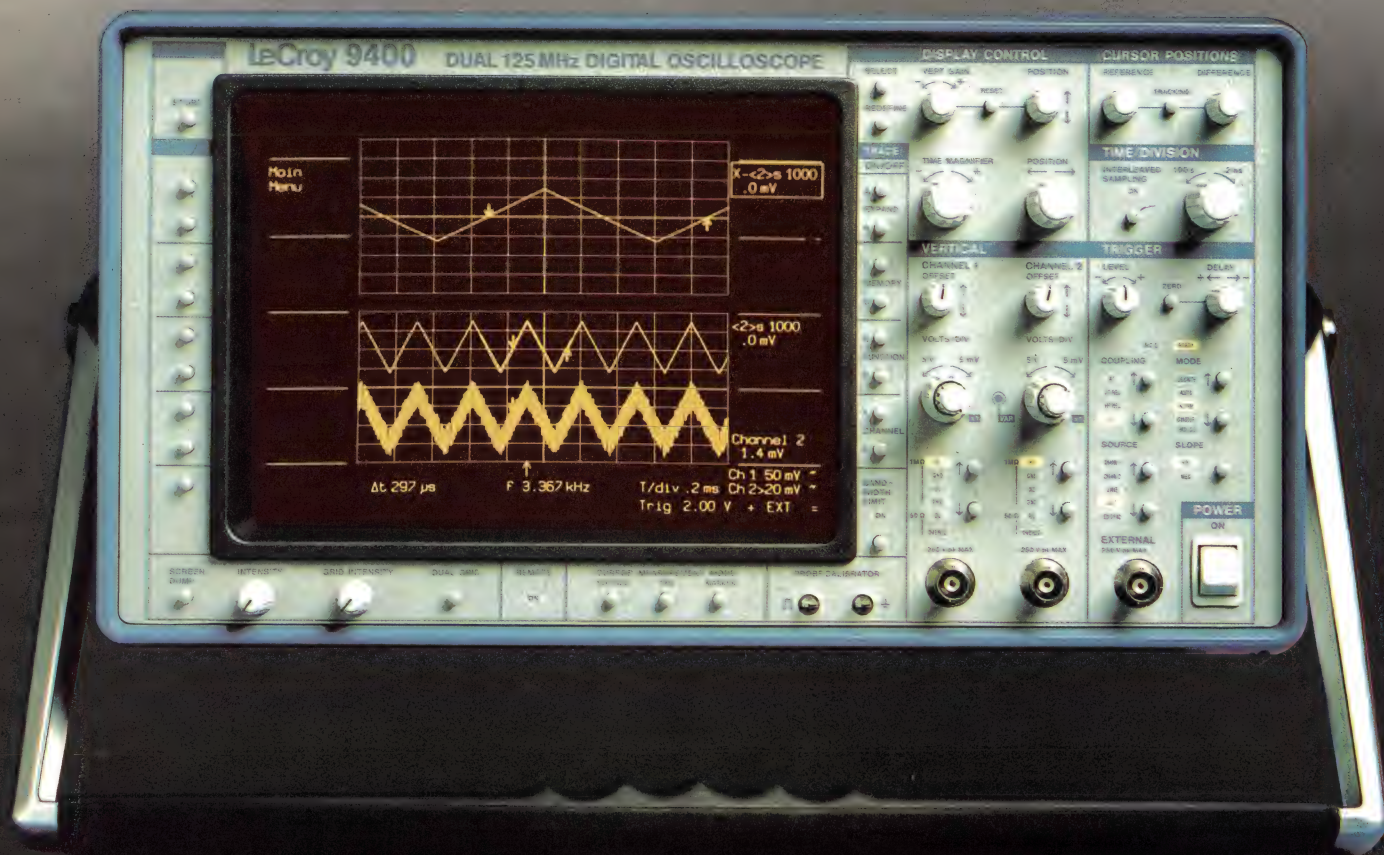
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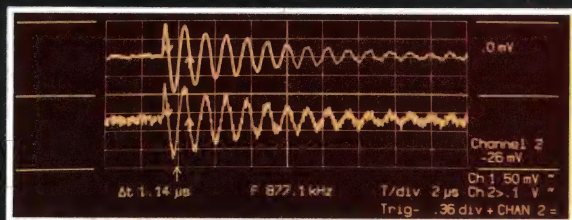
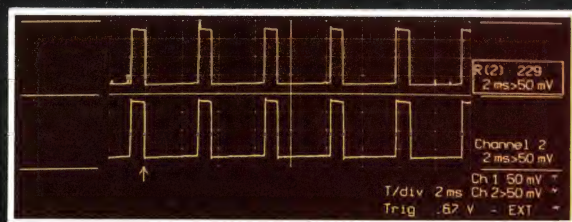
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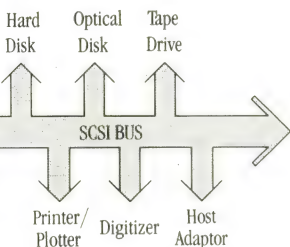
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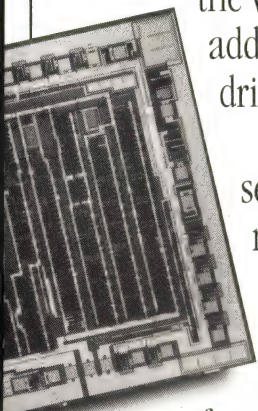
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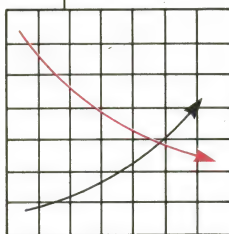
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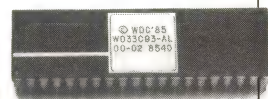
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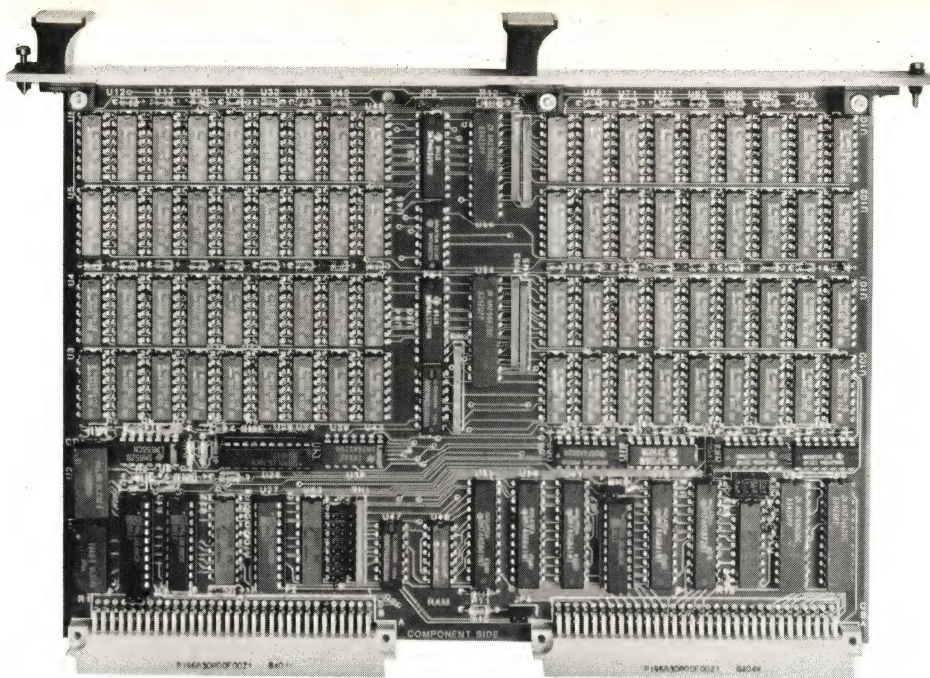
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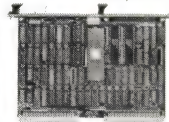
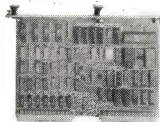
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- Speakers at ADEE East will offer practical solutions to CAE/CAD problems. Clay, Joanne, Staff Editor; *EDN*, 10/03/85, pg 85, 6 pgs.
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- Tool set links all stages of full-custom IC design. Staff; *Electronics*, 07/01/85, pg 60, 3 pgs.
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- Using programmable logic, desktop "foundry" lowers risk of semicustom design. Gladstone, Bruce, *FutureNet*; Ellis, William D, *Data I/O*; *Electronic Design*, 10/17/85, pg 143, 7.5 pgs.
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- Test chores and the PC: made for each other. Yates, Warren, Associate Editor; *Electronic Products*, 09/02/85, pg 66, 6 pgs.
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- At graphics conference, software tools will put on a brilliant display. Costlow, Terry, *Midwestern Editor*; *Electronic Design*, 07/11/85, pg 55, 2 pgs.
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- Custom-IC conference reflects significant gains for system designers. Weber, Samuel, *Semiconductor Editor*; *Electronics*, 05/20/85, pg 61, 4 pgs.
- Design conference sees AI lending a hand to automation tools. Milne, Bob, *Technology Editor*; *Electronic Design*, 06/13/85, pg 51, 2.66 pgs.
- European IC conference heralds the headway of non-CMOS processes. Beedie, Mitch, *European Editor*; *Electronic Design*, 08/22/85, pg 49, 4 pgs.
- International Test Conference zeroes in on RAMs and special-purpose memories. Milne, Bob, *Technology Editor*; *Electronic Design*, 10/31/85, pg 49, 3 pgs.
- Midcon/85 examines RISC influences on complex architectures. Patton, Carole, *East Coast Editor*; *Electronic Design*, 09/05/85, pg 53, 2.5 pgs.
- Multiple-processor systems and emerging architectures take the lead at NCC. Weiss, Ray, *West Coast Editor*; *Electronic Design*, 06/27/85, pg 51, 2.5 pgs.
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- Symposium reflects GaAs' growth, as new processes, structures evolve to complement its speed. Bursky, Dave, Associate Managing Editor; *Electronic Design*, 10/17/85, pg 57, 5 pgs.
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- Color-encoder LSI chip lights up TV screens. Scott, Ben, *Motorola*; Bergan, Marty, *Motorola*; *Electronic Products*, 05/01/85, pg 40, 6 pgs.
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- Data acquisition system plots relationships among vital variables. Jessen, Kenneth, *Hewlett-Packard*; *Electronic Design*, 10/31/85, pg 135, 4 pgs.
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Controller chip puts text and graphics on the same bit map. Carasso, Guido, Advanced Micro Devices, et al; *Electronic Design*, 06/27/85, pg 119, 7 pgs.

ECL chip set handles high-end display applications. Garbe, Olivier, Advanced Micro Devices; Reilly, Paul, Advanced Micro Devices; *Computer Design*, 07/15/85, pg 73, 5 pgs.

Flat-panel displays still chasing CRTs. Edwards, Sam, Contributing Editor; *Computer Design*, 10/01/85, pg 34, 4 pgs.

Highly integrated color palette chips burst on the scene. Goodenough, Frank, Technology Editor; *Electronic Design*, 08/08/85, pg 51, 4 pgs.

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2k \times 2k display scans eight beams in parallel. Williams, Tom, West Coast Managing Editor; *Computer Design*, 09/01/85, pg 40, 1 pg.

Focus on graphics workstations. Panasuk, Curtis, West Coast

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- Editor; Electronic Design, 08/22/85, pg 157, 7 pgs.*
Graphics Industry strives for new niches as mystique fades. *Manuel, Tom, Computers/Peripherals Editor; Electronics, 05/27/85, pg 59, 5 pgs.*
Graphics processing migrates from host to workstation. *Williams, Tom, West Coast Managing Editor; Computer Design, 07/15/85, pg 49, 9 pgs.*
Graphics systems deliver upfront performance. *Gustafson, Phil, Silicon Graphics; Computer Design, 07/15/85, pg 61, 5 pgs.*
Virtual windows speed color graphics displays. *Duydam, Jr, William E, Senior Editor; Computer Design, 08/15/85, pg 37, 1 pg.*
With a little help, high-quality graphics. *Husain, Rafe A, Graftek; Electronic Products, 09/16/85, pg 74, 8 pgs.*
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Chipmakers may keep ICE makers out in the cold. *Furlow, Bill, Senior Editor; Computer Design, 05/85, pg 41, 2.66 pgs.*
- Indicators**
Bright LEDs fill panel designers' palettes. *Chin, Spencer, Associate Editor; Electronic Products, 07/01/85, pg 38, 6.66 pgs.*
- Industrial electronics**
Automaker's MAP leads the way to factory automation. *Shapiro, Sydney F, Managing Editor; Computer Design, 05/85, pg 53, 6 pgs.*
Keep breadboard simple in hands-on DSP projects. *Cushman, Robert H, Special Features Editor; EDN, 09/05/85, pg 225, 10 pgs.*
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One supply powers precision bridge circuit. *Graeme, Jerry, Burr-Brown; EDN, 10/03/85, pg 207, 0.75 pgs.*
- Instrumentation/design aids & services/measurement, other**
Circuit measures fuse's rupture current. *Doraiswamy, TS, Motwane Manufacturing; EDN, 05/16/85, pg 232, 0.66 pgs.*
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Hardware tool streamlines software testing. *Ableidinger, Bruce, Northwest Instrument Systems; Computer Design, 10/01/85, pg 99, 5 pgs.*
PC-based analyzer links verification with software tools. *Gohsman, Gregory, Northwest Instrument; Computer Design, 08/15/85, pg 88, 6 pgs.*
Programmable translator turns multiple logic levels into a tester's TTL. *Kubota, Stanley P, Interface Technology; Electronic Design, 05/16/85, pg 177, 4 pgs.*
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Sensors and conditioning circuits simplify humidity measurement. *Sherman, Leonard H, National Semiconductor; EDN, 05/16/85, pg 179, 8.5 pgs.*
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- Integrated circuits/semiconductor devices/circuit design, other**
Armed with a battery of data, designers can reinforce MOSFET circuit reliability. *Clemente, Steve, International Rectifier, et al; Electronic Design, 06/06/85, pg 117, 6.5 pgs.*
Basic guidelines simplify designing for testability. *Cooper, Charles, Scientific Microsystems; Computer Design, 10/01/85, pg 77, 3 pgs.*
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Circuit provides temperature compensation. *Lutz, Joe, Peninsula Engineering; EDN, 06/13/85, pg 193, 1 pg.*
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Correlator IC speeds serial communication. *Yadagiri, Gunda, Isro Satellite Centre; EDN, 05/30/85, pg 282, 1 pg.*
Ending fourth decade, chip makers face doubt and upheaval.
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High-voltage CMOS ICs drive nonimpact printers. *Koehler, Chuck, Supertex; Electronic Products, 10/15/85, pg 75, 6 pgs.*
IC provides optimal lead-acid-battery charging cycles. *Valley, Rich, Unitrode; EDN, 10/31/85, pg 163, 13.5 pgs.*
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Market for speech ICs crumbles; software speech may fill the void. *Marrin, Ken, Senior Editor; Computer Design, 07/15/85, pg 19, 3.75 pgs.*
Mnics save space, increase reliability, and improve performance. *Lyman, Jerry, Packaging & Production Editor; Electronics, 05/20/85, pg 52, 6 pgs.*
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- Interconnection systems**
Shoring up the weak link in high-speed logic paths. *Staff; Electronics, 08/12/85, pg 46, 2 pgs.*
- Ion-implantation equipment**
Here comes a new breed of ION implanter. *Staff; Electronics, 09/09/85, pg 85, 3 pgs.*
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- K**
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Operate a computer's softkey remotely. *Fernando, Maurice, Times Fiber Communications; EDN, 08/22/85, pg 208, 1 pg.*
Two switches provide 7-state control. *Woellhaf, Jan, Ampex Switcher; EDN, 08/22/85, pg 206, 1 pg.*
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Making the LAN connection with a fiber optic standard. *Joshi, Sunil P, Advanced Micro Devices; Computer Design, 09/01/85, pg 64, 6 pgs.*
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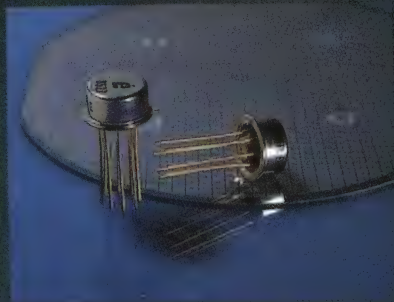
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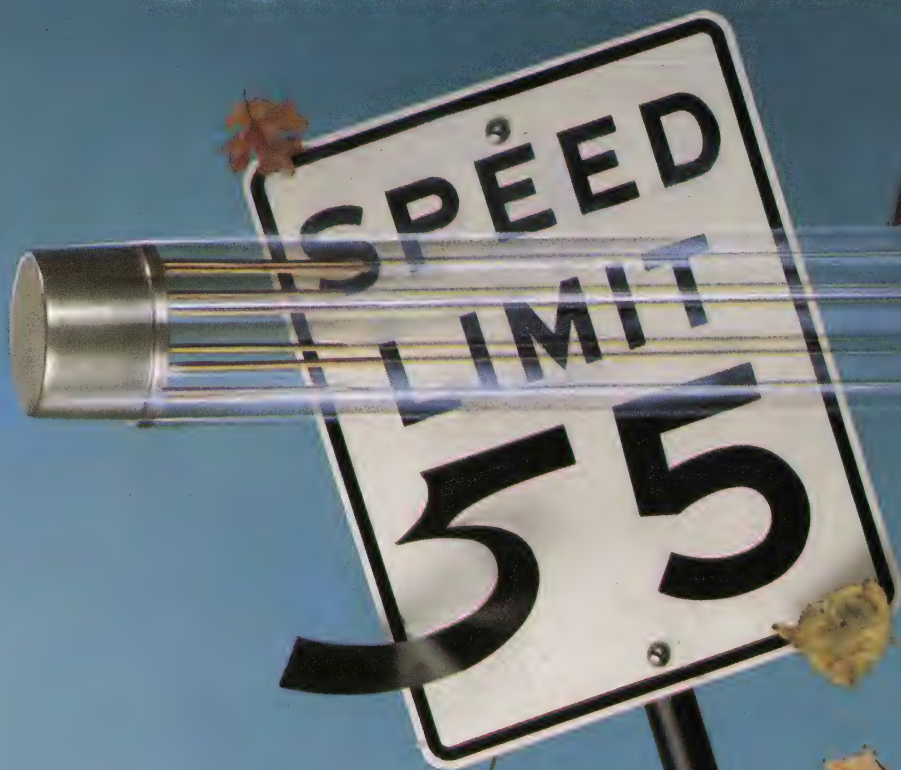
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Party line ties terminals without contention. Teeter, John, *Interface Product Planning*; Vesuna, Sarosh, *Advanced Micro Devices*; *Electronic Products*, 08/15/85, pg 37, 6 pgs.
The all-digital PBXs stake their claim on office automation. Rosenberg, Robert, *Systems Integration Editor*; *Electronics*, 05/06/85, pg 57, 5 pgs.

Logic analyzers/analysis

Analyzer module debugs 500-MHz logic with a scope's resolution. Damm, Wendell, *Tektronix*; *Electronic Design*, 08/22/85, pg 107, 5 pgs.
Logic analyzers offer wide choice of performance and price. Goering, Richard, *Field Editor*; *Computer Design*, 09/01/85, pg 25, 4 pgs.
With transitional timing, analyzers boost resolution, open wider windows. van Eijkelenburg, Herman, *Philips Test & Measuring Instruments*; *Electronic Design*, 08/15/85, pg 139, 7 pgs.

Logic arrays/systems

Create design files to simulate PLDs on a CAE workstation. Poniatowski, Martin, *Canaan Computer*; EDN, 09/19/85, pg 211, 6.5 pgs.
ECL PALs outpace their TTL equivalents. Marrin, Ken, *Senior Editor*; *Computer Design*, 07/01/85, pg 49, 2 pgs.
EPROM-based logic chip opens its gates to all flip-flop types, clocks. Hartmann, Robert, Altera; Wong, Sau-Ching, Altera; *Electronic Design*, 07/11/85, pg 109, 6.5 pgs.
FPLA interfaces 4-digit counter and μ P. Hartwig, Robert W, *Fairchild Camera and Instrument*; EDN, 08/08/85, pg 236, 0.5 pgs.
Input vectors drive simulation of logic-array designs. Franz, Michael, *Applied Micro Circuits*; EDN, 06/13/85, pg 153, 6.75 pgs.
Software savvy determines success in customizing PLDs. Schmitz, Nick, *Monolithic Memories*; Agahdel, Fairborz, *Signetics*; *Electronic Products*, 08/01/85, pg 70, 9 pgs.
Test software bolsters confidence level for programmable logic. Benson, Bjorn, *Data I/O*; Chi Siu, Denny, *Data I/O*; *Electronic Design*, 05/02/85, pg 161, 5.5 pgs.
Use simulation vectors to generate test vectors. Franz, Michael, *Applied Micro Circuits*; EDN, 06/27/85, pg 233, 6 pgs.
Using programmable logic, desktop "foundry" lowers risk of semicustom design. Gladstone, Bruce, *FutureNet*; Ellis, William D, *Data I/O*; *Electronic Design*, 10/17/85, pg 143, 7.5 pgs.

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Mask-aligning/exposure equipment

A new mask could finally open up X-ray lithography. Staff; *Electronics*, 09/16/85, pg 48, 3 pgs.

Mask-making equipment, photorepeating/replication

Laser beams speed up reticle writing. Staff; *Electronics*, 10/07/85, pg 40, 3 pgs.

Materials research/development

Symposium reflects GaAs' growth, as new processes, structures evolve to complement its speed. Bursky, Dave, *Associate Managing Editor*; *Electronic Design*, 10/17/85, pg 57, 5 pgs.

Memory boards/systems

Benchmarks contrast 68020 cache-memory operations. Ripps, David, *Industrial Programming*; Mushinsky, Bernard, *Industrial Programming*; EDN, 08/08/85, pg 177, 6.5 pgs.
DMA cache speeds execution in mixed-bus systems. Tehranian, Michael M, *Digital Equipment*; *Computer Design*, 07/15/85, pg 85, 4 pgs.
Memory management boosts efficiency of powerful micros. Tomplait, Cliff, *Texas Instruments*; *Computer Design*, 07/01/85, pg 105, 4.5 pgs.
Twin cache tags enable concurrent micro/DMA processing. Tehranian, Michael M, *Digital Equipment*; *Computer Design*, 06/85, pg 157, 3 pgs.

Memory controllers

Twin cache tags enable concurrent micro/DMA processing. Tehranian, Michael M, *Digital Equipment*; *Computer Design*, 06/85, pg 157, 3 pgs.

Memory devices

CMOS 256-kbit video RAM, with wide two-way bus, picks up speed, drops power. Price, Simon M, *Advanced Micro Devices*; *Electronic Design*, 09/19/85, pg 171, 5.5 pgs.
CMOS 64k RAM mates static speed with dynamic density. EDN January 9, 1986

Bagnall, Peter, *VISIC*; Furnweger, Charles, *VISIC*; *Electronic Design*, 07/25/85, pg 117, 6 pgs.

Different personalities lend shadow RAM a range of operating modes. Woodruff, Bill, *Mostek*; *Electronic Design*, 09/19/85, pg 183, 5 pgs.

Dynamic video RAM snaps the bond between memory and screen refresh. Forman, Steve, *NEC Electronics*; *Electronic Design*, 05/30/85, pg 117, 6 pgs.

EEPROM technology seeds reprogrammable logic. Staff; *Electronics*, 06/03/85, pg 56, 2 pgs.

Focus on high-speed static RAMs. Costlow, Terry, *Midwestern Editor*; *Electronic Design*, 09/19/85, pg 223, 7 pgs.

High-speed FIFOs contend with widely differing data rates. Miller, Michael J, *Integrated Device Technology*; Toth, Frank L, *Integrated Device Technology*; *Computer Design*, 09/01/85, pg 83, 4 pgs.

International Test Conference zeroes in on RAMs and special-purpose memories. Milne, Bob, *Technology Editor*; *Electronic Design*, 10/31/85, pg 49, 3 pgs.

"Keep it simple" is 1-Mbit ROM's motto for μ P interfaces. Linden, Jeff, *Mostek*; Laverdier, John, *Mostek*; *Electronic Design*, 06/13/85, pg 171, 4 pgs.

Large disk cache uses fast 64k-by-1 static RAMs to speed data-base accesses. Hartwig, Robert, et al; *Electronic Design*, 09/19/85, pg 193, 8 pgs.

Makers drop their prices in bid to avert pileup of 256-Kbit DRAMs. Myrvaagnes, Rodney, *Associate Editor*; *Electronic Products*, 09/02/85, pg 46, 5 pgs.

Memory chips take application-specific IC route. Mokhoff, Nicolas, *Senior Editor*; *Computer Design*, 08/01/85, pg 23, 3.66 pgs.

Once a difficult task, bubble memory design is now a question of layout. Knapp, Steven, *Intel*; *Electronic Design*, 08/15/85, pg 157, 4.5 pgs.

Standard-cell ICs and gate arrays integrate memory systems on chip. Smith, David, *Associate Editor*; EDN, 10/03/85, pg 59, 5 pgs.

Switch lets you select memory devices. Ahmad, M O, *Concordia University*; Poorniah, D V, *Concordia University*; EDN, 07/25/85, pg 312, 1.5 pgs.

Test designers challenged by a new generation of CMOS dynamic RAMs. Stensland, Robert W, *Intel*; *Electronic Design*, 06/06/85, pg 101, 6.5 pgs.

Use simple circuits, algorithms to program 512k-bit EPROMs. Robinson, Kurt, *Intel*; EDN, 08/22/85, pg 163, 6 pgs.

VLSI dynamic RAM components. Staff; *Electronic Design*, 08/15/85, pg 167, 10 pgs.

Variety, versatility make nonvolatile memory difficult to forget. Sommers, Ron, *Electronic Design*, 06/06/85, pg 78, 14 pgs.

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Intel launches two 80386-based Multibus-board computers. Mokhoff, Nicolas, *Senior Editor*; *Computer Design*, 10/15/85, pg 27, 2.5 pgs.

Intelligent interfaces enhance STD bus systems. Phillip, Chuck, *United Technologies*; EDN, 09/05/85, pg 201, 14 pgs.

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Multibus II and VMEbus compete for realtime applications. Marrin, Ken, *Senior Editor*; *Computer Design*, 08/15/85, pg 24, 2.5 pgs.

Multibus II makes headway in realtime applications. Shapiro, Sydney F, *Managing Editor*; *Computer Design*, 07/01/85, pg 35, 2.65 pgs.

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Circuit links asynchronous μP with 6522. *Boukadoum, A Mounir, Université du Quebec; EDN, 06/27/85, pg 242, 1 pg.*
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Floating-point chip set beefs up desktop systems with processing muscle. *White, George, Weitek; Sackett, Brian, Weitek; Electronic Design, 05/30/85, pg 107, 7 pgs.*

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146805 μP addresses an extra 10k bytes. *Hardway, Jay, Keithly Instruments; EDN, 09/05/85, pg 303, 1.33 pgs.*
32-bit μP is a fine match for today's languages and operating systems. *Agarwal, Rakesh, Intel, et al; Electronic Design, 10/31/85, pg 161, 7.5 pgs.*
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32-bit microprocessor can run Unix and MS-DOS programs concurrently. *Keating, Timothy J, Intel, et al; Electronic Design, 10/17/85, pg 115, 7 pgs.*
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Full duplex, 2400-baud, dial-up modems moving to chip level. *Marrin, Ken, Senior Editor; Computer Design, 10/15/85, pg 56, 3.5 pgs.*
Hybrid module simplifies intelligent-modem integration. *Durham, Stephen J, Cermetek Microelectronics; Electronic Products, 07/01/85, pg 56, 6 pgs.*
Modem standards aimed at modern transmission schemes. *Repko, Marya, Bootstrap; Computer Design, 08/01/85, pg 119, 2.65 pgs.*
Single-chip modem provides low-cost data communication. *Lee, Wesley, National Semiconductor; EDN, 10/31/85, pg 189, 7.5 pgs.*
Smart 2400-bps modems use error-reduction and -correction schemes for data integrity. *Terry, Chris, Associate Editor; EDN, 09/19/85, pg 83, 4.5 pgs.*
Use controller and chips to design an intelligent modem. *Chirayil, Raj, Texas Instruments; Gammon, Robert, Texas Instruments; EDN, 05/02/85, pg 213, 7 pgs.*

Modular instruments

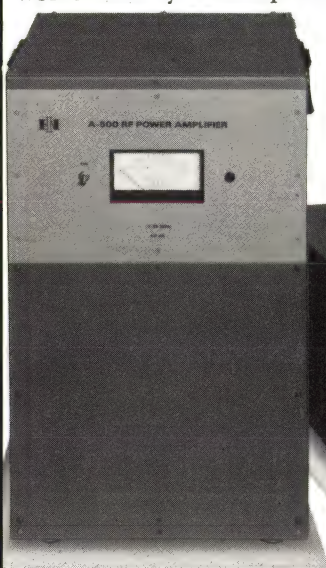
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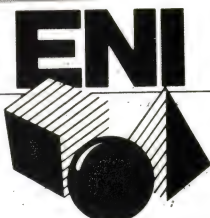
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Richard, Field Editor; *Computer Design*, 10/01/85, pg 42, 2.5 pgs.

Monitor circuits

Circuit monitors power-supply current. Kirby, Steve, *Analog Devices*; *EDN*, 05/16/85, pg 228, 1 pg.

Motor control circuits

Brushless dc motors get a controller IC that replaces complex circuits. de Sa e Silva, Claudio, *Unitrode Integrated Circuits*; *Electronic Design*, 09/19/85, pg 149, 6 pgs.

Control a bidirectional 4 ϕ stepper motor. Lakshminarayanan, V., *Government of India*; *EDN*, 09/05/85, pg 306, 1.5 pgs.

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Sophisticated controller ICs adapt motors to robotics and computer-peripheral applications. Teja, Ed, *Western Editor*; *EDN*, 10/17/85, pg 49, 5 pgs.

Switched-mode controller targets motors. de Sa e Silva, Claudio, *Unitrode*; *Electronic Products*, 06/17/85, pg 85, 7 pgs.

Motors/motor controllers

Focus on stepper motors. Costlow, Terry, *Technology Editor*; *Electronic Design*, 10/31/85, pg 183, 6 pgs.

Multiplexers/concentrators

Circuit creates programmable time window. Lubs, Steve, *Department of Defense*; *EDN*, 10/03/85, pg 202, 1.33 pgs.

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Computers. Manuel, Tom, *Senior Editor*; *Electronics*, 10/07/85, pg 49, 4 pgs.

Concurrent computers ideal for inherently parallel problems. Asbury, Ray, *Intel*; *Computer Design*, 09/01/85, pg 99, 6.5 pgs.

Distributed supermicro architectures tackle computationally intensive chores. Teja, Edward R, *Western Editor*; *EDN*, 05/02/85, pg 51, 3 pgs.

For hefty computing power, European designers flex multiprocessor muscle. Ohr, Stephan, *Technology Editor*; *Electronic Design*, 07/25/85, pg 57, 3 pgs.

Multiple-processor systems and emerging architectures take the lead at NCC. Weiss, Ray, *West Coast Editor*; *Electronic Design*, 06/27/85, pg 51, 2.5 pgs.

Multiprocessing superminicomputers handle Unix demands. Killmon, Peg, *Senior Editor*; *Computer Design*, 08/15/85, pg 22, 2 pgs.

Multiprocessor makes parallelism work. Staff; *Electronics*, 09/02/85, pg 46, 3 pgs.

Multiprocessor computers expand user vistas. Siewiorek, Daniel P., *Carnegie Mellon University*, et al; *Computer Design*, 08/15/85, pg 70, 5.75 pgs.

Multi-user micro preserves familiar environment. Siegel, Herbert L., *Action Computer Enterprise*; Barbier, Ken, *Action Computer Enterprise*; *Computer Design*, 05/85, pg 147, 5 pgs.

Parallel machine expands indefinitely. Manuel, Tom, *Senior Editor*; *Electronics*, 05/13/85, pg 49, 5 pgs.

Software opens the way to true concurrency for multiprocessing. Patton, Carole, *East Coast Editor*; *Electronic Design*, 08/08/85, pg 83, 7 pgs.

Supermicros mount strong challenge to mid-range systems. Killmon, Peg, *Senior Editor*; *Computer Design*, 10/01/85, pg 23, 3.5 pgs.

The transputer spawns a radically new computer. Staff; *Electronics*, 10/07/85, pg 43, 3 pgs.

Multiuser computer systems

High-performance microcomputers. Mosley, J D, *Associate Editor*; Clay, Joanne, *Staff Editor*; *EDN*, 10/03/85, pg 125, 9 pgs.

Multi-user micro preserves familiar environment. Siegel, Herbert L., *Action Computer Enterprise*; Barbier, Ken, *Action Computer Enterprise*; *Computer Design*, 05/85, pg 147, 5 pgs.

Harvey J, *Special Features Editor*; *Computer Design*, 06/85, pg 69, 4.75 pgs.

Ethernet chips are cheap, but cabling still costly. Marrin, Ken, *Senior Editor*; *Computer Design*, 10/15/85, pg 55, 1 pg.

Here at last: TI's chip set for the IBM token-ring net. Staff; *Electronics*, 10/21/85, pg 56, 4 pgs.

MAP chips become commercially available. Marrin, Ken, *Senior Editor*; *Computer Design*, 10/15/85, pg 50, 1 pg.

Manchester-code IC handles network's physical link. Moseley, Gerald, *Seeq Technology*; *EDN*, 05/30/85, pg 163, 11 pgs.

Protocol controller chip manages X.25 interface. Erickson, Ivan, *Motorola*; *Computer Design*, 09/01/85, pg 78, 4 pgs.

Smart chip outperforms FIFOs in network adapters. Shin, Paul, *Texas Instruments*; Koontz, Jerry, *Texas Instruments*; *Computer Design*, 05/85, pg 155, 5 pgs.

Network architecture/design/design standards (nonlocal)

As the age of ISDN nears, thorny technical issues still await resolution. Allan, Roger, *Technology Editor*; *Electronic Design*, 06/27/85, pg 63, 2 pgs.

IBM's SNA enhancements start to generate compatible products. Mokhoff, Nicolas, *Senior Editor*; *Computer Design*, 07/15/85, pg 27, 2 pgs.

Integrated Services Digital Network sparks VLSI telecomm-IC explosion. Cormier, Denny, *Western Editor*; *EDN*, 05/30/85, pg 63, 9 pgs.

Updates to SNA change system network rules. Czubek, Donald H., *Communications Solutions*; *Computer Design*, 09/01/85, pg 72, 4 pgs.

O

Op amps

Analog circuits operate from a 1.5V cell. Williams, Jim, *Linear Technology*; *EDN*, 09/19/85, pg 195, 11 pgs.

Design linear circuits for 5V operation. Williams, Jim, *Linear Technology*; *EDN*, 05/02/85, pg 163, 12 pgs.

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Operational amplifiers. Travis, Bill, *Senior Editor*; *EDN*, 05/16/85, pg 118, 24.5 pgs.

Power op amps simplify drive-circuit design tasks. Lutz, Ronald W., *Sprague Electric*; Dewey, F Raymond, *Sprague Electric*; *EDN*, 08/22/85, pg 147, 9 pgs.

Precision op amp ends concessions in speed, noise, and dc performance. Hansford, Alan, *Harris Semiconductor*; Reimer, David, *Harris Semiconductor*; *Electronic Design*, 10/03/85, pg 115, 5 pgs.

Optical character readers

Bar-code readers and scanners meet diverse data-collection requirements. Terry, Chris, *Associate Editor*; *EDN*, 10/17/85, pg 61, 5.66 pgs.

Optical storage

Erasable optical disks are on the horizon. Staff; *Electronics*, 06/24/85, pg 67, 3 pgs.

Magneto-optics combines erasability and high-density storage. Ohr, Stephan, *Technology Editor*; *Electronic Design*, 07/11/85, pg 93, 7 pgs.

Optical disk drives in controversy over file updates. Williams, Tom, *West Coast Managing Editor*; *Computer Design*, 08/15/85, pg 30, 1.33 pgs.

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Optoelectronics

Coming in at 20 Mbaud, an optocoupler IC doubles the data transfer rate. Slawson, Michael R, *Hewlett-Packard*; *Electronic Design*, 10/03/85, pg 133, 4 pgs.

Oscillators

Crystal oscillator sets pulse width. Barnett, T G, *London Hospital Medical College*; *EDN*, 08/08/85, pg 244, 1 pg.

Oscilloscopes

50 to 100-MHz oscilloscopes a great buy. Yates, Warren, *Associate Editor*; *Electronic Products*, 10/15/85, pg 43, 3 pgs.

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N

Network analyzers/analysis

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Networking ICs

Chip sets forge vital links for token bus networks. Hindin, *EDN* January 9, 1986

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P

Parallel processing

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Computer architectures: Varied blueprints will lift system speeds to dizzying heights. *Weiss, Ray, West Coast Editor; Electronic Design, 05/30/85, pg 82, 7 pgs.*
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Parallel processing promises faster program execution. *Hindin, Harvey J, Special Features Editor; Computer Design, 08/15/85, pg 57, 9.75 pgs.*
Parallel-processing computer overcomes memory contention. *Chang, Robin, International Parallel Machines; Computer Design, 09/15/85, pg 113, 4 pgs.*
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Peak detectors

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Graphics card choice depends on compatible software. *Wright, Maury, Western Editor; EDN, 07/25/85, pg 56, 8 pgs.*
Helping change how engineers design. *Gabay, Jon, Associate Editor; Electronic Products, 09/02/85, pg 57, 6 pgs.*
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Plastics/resins

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Pots/trimmers

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Power semiconductors

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Power diodes save ICs from early death. *Brokaw, Paul, Analog Devices; Electronic Products, 10/15/85, pg 61, 4.5 pgs.*
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Circuits eliminate power-supply surge currents. *Sokal, Nathan, Design Automation; EDN, 09/05/85, pg 141, 5 pgs.*
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Three-rail power supply uses four diodes. *de Sa, Luis, Universidade de Coimbra; EDN, 10/31/85, pg 248, 0.66 pgs.*
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Printed circuits

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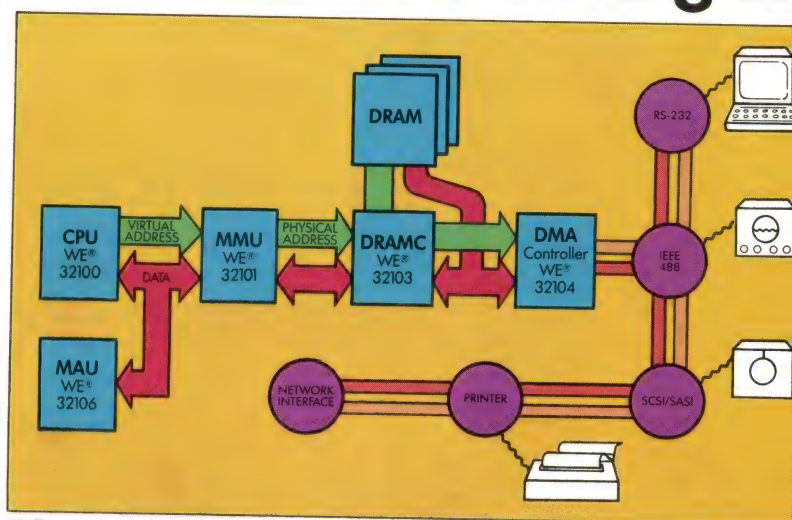
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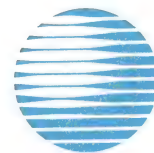
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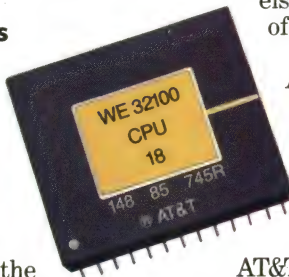
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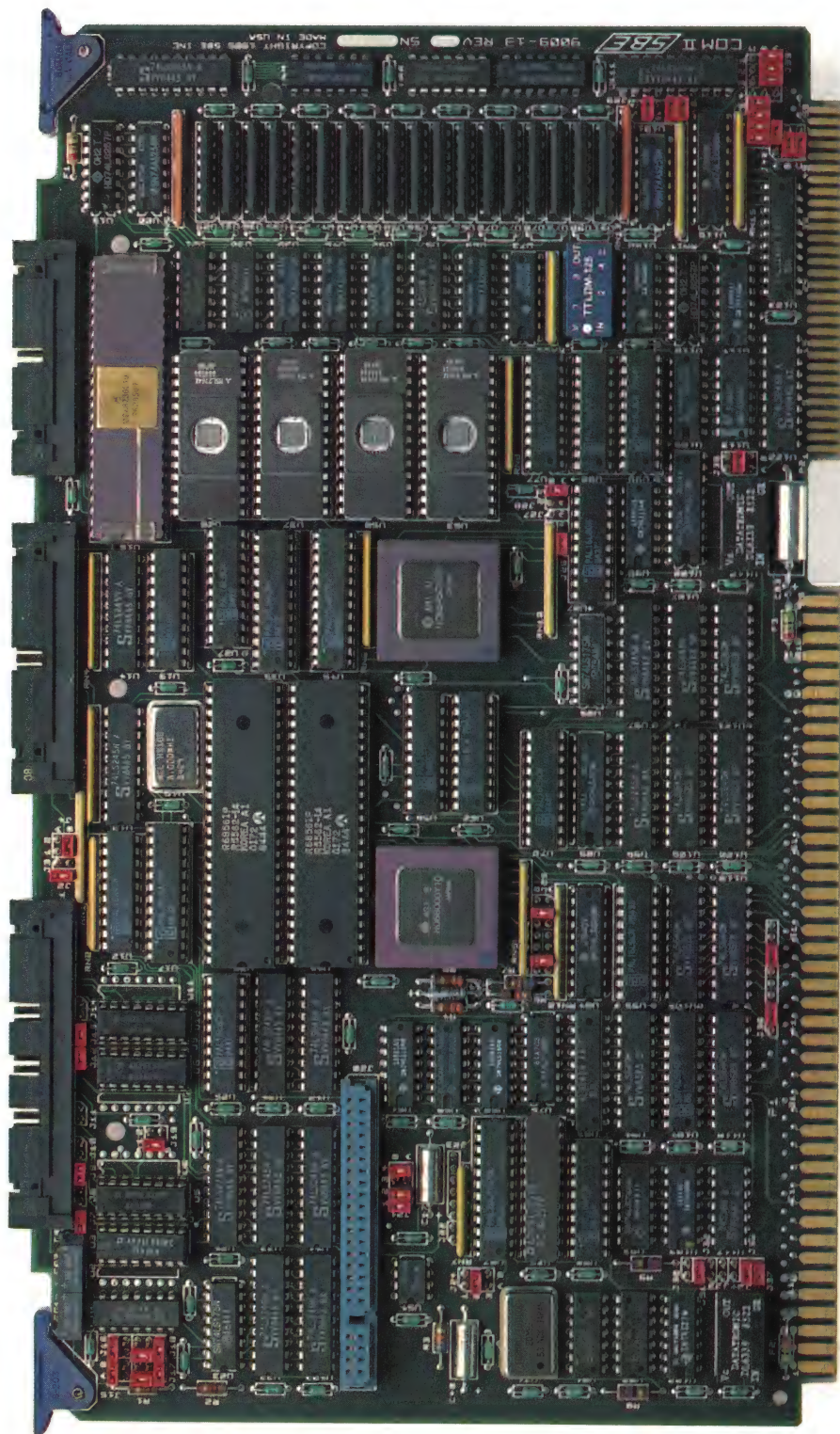
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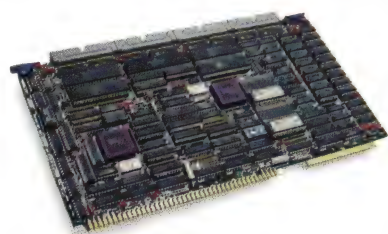
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EDN TECHNICAL-ARTICLE DATABASE

Printer controllers

Controller sets the pace for laser printing. *Carter III, James M, Quality Micro Systems, et al; Electronic Products, 09/02/85, pg 62, 5 pgs.*

Printer-control code set promises programming ease. *Seki, Haruyuki, Epson; EDN, 09/05/85, pg 167, 3.85 pgs.*

Trade-off analysis eases design of print controller. *Carrington, J E, IBM Development Lab; Westcott, G R, IBM Development Lab; Computer Design, 07/01/85, pg 135, 4 pgs.*

Printers

Controller sets the pace for laser printing. *Carter III, James M, Quality Micro Systems, et al; Electronic Products, 09/02/85, pg 62, 5 pgs.*

Imagery stands out in nonimpact printing. *Rumsey, John, Delphax Systems; Electronic Products, 09/02/85, pg 69, 6 pgs.*

Private branch exchanges (PBXs)

The all-digital PBXs stake their claim on office automation. *Rosenberg, Robert, Systems Integration Editor; Electronics, 05/06/85, pg 57, 5 pgs.*

Probing systems/accessories

Understand probe resistance to ensure accurate measurements. *Escovitz, William, Hewlett-Packard; EDN, 06/13/85, pg 187, 4 pgs.*

Processors, special-purpose (array, front-end, etc)

Accelerate your PC's arithmetic with an array processor. *Tetewsky, Avram K, Draper Laboratory; EDN, 10/03/85, pg 155, 7.75 pgs.*

Performance, not promises, dispels megaflops myth. *Schrage, Martin, CSP; Computer Design, 09/15/85, pg 92, 4 pgs.*

Rounded-off bits behave like noise sources. *Frisch, Bob, Mercury Computer Systems; Electronic Products, 05/15/85, pg 79, 4 pgs.*

Production testing techniques

Military takes steps to oust poor ICs from defense systems. *Walters von Alten, Judith, Northwestern Editor; Electronic Products, 10/01/85, pg 53, 4 pgs.*

Production/manufacturing/testing, other

Basic guidelines simplify designing for testability. *Cooper, Charles, Scientific Microsystems; Computer Design, 10/01/85, pg 77, 3 pgs.*

Digital test system attacks the evaluation of VLSI prototypes. *Pollard, Gary, Hilevel Technology; Masters, Tom, Hilevel Technology; Electronic Design, 08/08/85, pg 95, 7 pgs.*

Testing, fault tolerance emerge as top issues at wafer-scale conference. *Beebie, Mitch, European Editor; Electronic Design, 07/11/85, pg 63, 2 pgs.*

Programming

Fast subroutine calculates exponentials. *Grappel, Robert D, MIT Lincoln Laboratory; EDN, 05/02/85, pg 231, 1 pg.*

New C programming tools emphasize debugging capabilities. *Suydam, William E, Senior Editor; Computer Design, 05/85, pg 48, 1 pg.*

Numerical sort requires no user program. *Martin, Robert, Frequency Engineering Labs; EDN, 05/30/85, pg 284, 0.5 pgs.*

Program converts Gray to binary and back. *Grappel, Robert, MIT Lincoln Laboratory; EDN, 05/30/85, pg 286, 0.5 pgs.*

Program provides gray-binary conversion. *Sporea, Dan G, Central Institute of Physics; EDN, 06/13/85, pg 196, 1.5 pgs.*

Program simplifies number format. *Maresca, T J, EDN, 09/19/85, pg 246, 0.75 pgs.*

Programs perform decimal/octal conversion. *Pohedra, Joe, Harris; EDN, 06/27/85, pg 248, 0.85 pgs.*

Simple routines provide calendar date. *Grappel, Robert D, MIT Lincoln Laboratory; EDN, 10/17/85, pg 168, 1 pg.*

Single instruction speeds I/O transfers. *Mugioiu, Florin N, Institute for Electronic Research; EDN, 05/30/85, pg 284, 0.5 pgs.*

Single-line program gives multiple delays. *Dart, Andrew, Trans-Texas Telegraph; EDN, 05/02/85, pg 232, 0.5 pgs.*

Software prevents false interrupts. *Sporea, Dan G, Central Institute of Physics; EDN, 08/22/85, pg 212, 1.5 pgs.*

Software routine prevents stack overflow. *Ehrecke, Richard J, Microcomputer Memories; EDN, 09/05/85, pg 304, 1 pg.*

PROM programmers/programming

Focus on universal device programmers. *Costlow, Terry, Midwestern Editor; Electronic Design, 05/30/85, pg 141, 5.5 pgs.*

Use simple circuits, algorithms to program 512k-bit EPROMs. *Robinson, Kurt, Intel; EDN, 08/22/85, pg 163, 6 pgs.*

Pulse generators/generation/detection

Adjustable delay can exceed 360°. *Engle, James L, University of Pennsylvania; EDN, 10/03/85, pg 204, 1 pg.*

Benchmark pulse generators address high-speed applications. *Small, Charles H, Associate Editor; EDN, 07/25/85, pg 135, 6 pgs.*

Detect out-of-bound pulse widths. *Sukh Jain, Dil, Nat'l Remote Sensing Agency; EDN, 09/19/85, pg 242, 0.75 pgs.*

Modulator offers 12-bit precision. *Valliant, H D, Dept of Energy, Mines, and Resources; Gagnon, C, Dept. of Energy, Mines, and Resources; EDN, 06/27/85, pg 244, 1 pg.*

Vary frequency without changing duty cycle. *Rogers, Gordon, EDN, 06/13/85, pg 199, 0.5 pgs.*

Pulse-width modulators

PWM controller chip hits frequency highs of switching supplies. *Wofford, Larry, Unitrode Integrated Circuits; Electronic Design, 05/30/85, pg 97, 6 pgs.*

R

Regulators

Current-sensing IC improves regulation of power supplies. *Fritz, Glenn, Unitrode; Wofford, Larry, Unitrode; Electronic Products, 06/17/85, pg 77, 6 pgs.*

Novel designs ensure that linear regulator ICs remain up-to-date. *Heftman, Gene, Electronic Design, 08/15/85, pg 39, 4 pgs.*

Tracking-load bank tests bipolar supplies. *Bley, David B, Chattanooga; EDN, 10/31/85, pg 252, 0.66 pgs.*

Relays

Beyond usual specs is a path to better relays. *Bishop, Anthony, International Rectifier; Electronic Products, 08/01/85, pg 60, 6 pgs.*

Despite sleepy image, relay technology makes strides forward. *Rand, Michael B, Components Editor; Electronics, 06/10/85, pg 39, 4 pgs.*

Resistors

Surface mounting shrinks resistor networks. *Chin, Spencer, Associate Editor; Electronic Products, 08/15/85, pg 51, 5 pgs.*

Using improved materials, precision resistors set performance records. *Winard, Harold, Associate Editor; Electronic Design, 06/06/85, pg 58, 3 pgs.*

Rigid-disk drives

Analyzing risks is key to high-performance. *Klonick, John R, Maxtor; Electronic Products, 06/17/85, pg 61, 4 pgs.*

Data-compression techniques ease storage problems. *Bray, John M, Auburn University, et al; Computer Design, 10/15/85, pg 102, 5 pgs.*

Decoding specs comes first in choosing a Winchester. *Anderson, Roger W, Consultant's Choice; Electronic Products, 06/17/85, pg 54, 4.66 pgs.*

Focus on high-capacity winchester disk drives. *Ohr, Stephan, Technology Editor; Electronic Design, 09/19/85, pg 209, 6 pgs.*

Magneto-optics combines erasability and high-density storage. *Ohr, Stephan, Technology Editor; Electronic Design, 07/11/85, pg 93, 7 pgs.*

Storage peripherals adapt to new demands for speed and capacity. *Killmon, Peg, Senior Editor; Computer Design, 05/85, pg 83, 10 pgs.*

Sub-4-in. Winchester disk drives. *Teja, Edward R, Western Editor; EDN, 06/27/85, pg 117, 6 pgs.*

Thin-film sputtering will overtake plating for Winchester disks. *Ohr, Stephan, Technology Editor; Electronic Design, 09/15/85, pg 100, 7 pgs.*

Winchester drives face critical problems in design and testing. *Lieberman, David, Associate Editor; Electronic Products, 06/03/85, pg 40, 10 pgs.*

Robotics

At robotics conference, factory software will prove that it is up to the job. *Costlow, Terry, Midwestern Editor; Electronic Design, 05/30/85, pg 51, 2 pgs.*

Electronic factories gearing up for industrial robots. *Walters von Alten, Judith, Northwestern Editor; Electronic Products, 05/15/85, pg 40, 7 pgs.*

Microcontrollers offer realtime robotics control. *Horden, Ira, Intel; Computer Design, 10/15/85, pg 98, 4 pgs.*

Robots and microprocessor mix well. *Melear, Charlie, Motorola; Electronic Products, 06/17/85, pg 68, 8 pgs.*

S

Scientific computer systems

High-performance microcomputers. *Mosley, J D, Associate Editor; Clay, Joanne, Staff Editor; EDN, 10/03/85, pg 125, 9 pgs.*

Minicomputer takes simple route to speed Unix. *Killmon, Peg, Senior Editor; Computer Design, 06/85, pg 33, 2.66 pgs.*

Vector architectures make supercomputing affordable. *Killmon, Peg, Senior Editor; Computer Design, 09/01/85, pg 32, 2.66 pgs.*

Semicustom/custom ICs

2- μ m standard-cell family builds VLSI semicustom circuits. *Petrizzo, Susan, Texas Instruments; Electronic Design, 06/13/85, pg 123, 5.5 pgs.*

A chip business that is still growing. *Conrad Cole, Bernard, Electronics, 07/22/85, pg 40, 6 pgs.*

Application-specific ICs, relying on RAM, implement almost any logic function. *Landry, Steve, Xilinx; Electronic Design, 10/31/85, pg 123, 7 pgs.*

Bipolar array IC builds high-voltage analog circuits nearing gigahertz speeds. *Metcalf, Mike, Tektronix; Electronic Design, 09/05/85, pg 169, 4 pgs.*

CAD kit switches gate-array design from foundry to workstation. *Friedman, Michael, Gould AMI Semiconductors; Hampton, Lisa, Mentor Graphics; Electronic Products, 10/15/85, pg 68, 5.33 pgs.*

Channelless structure pushes back density limits of CMOS standard cells. *Martin, Jaime, California Devices, et al; Electronic Design, 06/13/85, pg 147, 6 pgs.*

Design gate arrays using an enhanced personal computer. *Basson, Mike, FutureNet; Saal, Fred, Hughes Aircraft; EDN, 05/30/85, pg 207, 8 pgs.*

Design tool vendors move toward integrated systems. *Goering, Richard, Field Editor; Computer Design, 06/85, pg 103, 13 pgs.*

Distinctions blur between gate arrays and cells as digital technology evolves. *Bursky, Dave, Technology Editor; Electronic Design, 06/13/85, pg 81, 5.33 pgs.*

Gallium arsenide challenges silicon in high-speed-array applications. *Smith, David, Associate Editor; EDN, 06/27/85, pg 75, 3.5 pgs.*

Grading test vectors: Ingenuity adds polish to brute force. *Milne, Bob, Technology Editor; Electronic Design, 08/22/85, pg 87, 7.5 pgs.*

Hardware modeling eases simulation of complex chips. *Williams, Tom, West Coast Managing Editor; Computer Design, 05/85, pg 33, 3.66 pgs.*

Here comes a do-it-yourself silicon compiler. *Staff; Electronics, 10/14/85, pg 50, 2 pgs.*

How gate arrays are keeping ahead. *Conrad Cole, Bernard, Electronics, 09/23/85, pg 43, 5 pgs.*

ICCD stresses methods that speed and simplify the VLSI design process. *Patton, Carole, East Coast Editor; Electronic Design, 10/03/85, pg 53, 3 pgs.*

Is semicustom effective for military needs? *Gabay, Jon, Associate Editor; Electronic Products, 10/01/85, pg 61, 3 pgs.*

LSI-level standard cells form the core of integrated μ P and peripheral systems. *Smith, David, Associate Editor; EDN, 08/22/85, pg 75, 6 pgs.*

Megacells: A faster route to semicustom chip design. *Staff; Electronics, 07/15/85, pg 56, 2.5 pgs.*

New standard cells provide integration options. *Dondale, Steve, NCR Microelectronics; Zwetzig, Randy, NCR Microelectronics; EDN, 10/17/85, pg 143, 5 pgs.*

Powerful PC-based tools close the loop between designing and testing ICs. *Gladstone, Bruce, FutureNet; Westerhoff, Todd, HHB-Softtron; Electronic Design, 06/13/85, pg 159, 7 pgs.*

Standard cells step in to ease the design of high-voltage chips. *Shackle, Peter W, Telmos; Electronic Design, 09/05/85, pg 149, 5 pgs.*

Standard-cell ICs and gate arrays integrate memory systems on chip. *Smith, David, Associate Editor; EDN, 10/03/85, pg 59, 5 pgs.*

Understand the limits of passive analog IC components. *Ritmanich, Will, Barvon Research; EDN, 10/17/85, pg 155, 4 pgs.*

Using programmable logic, desktop "foundry" lowers risk of semicustom design. *Gladstone, Bruce, FutureNet; Ellis, William D, Data I/O; Electronic Design, 10/17/85, pg 143, 7.5 pgs.*

Sensors/transducers

Nonvision sensors. *Allan, Roger, Special Features Editor; Electronic Design, 06/27/85, pg 103, 6.5 pgs.*

Precision sensors bring intelligence to assembly robots. *Schreiner, L L, Intellex; Computer Design, 08/01/85, pg 85, 5 pgs.*

Sensors and conditioning circuits simplify humidity measurement. *Sherman, Leonard H, National Semiconductor; EDN, 05/16/85, pg 179, 8.5 pgs.*

Signal sources/generation

Design techniques extend V/F-converter performance. *Williams, Jim, Linear Technology Corp; EDN 05/16/85, pg 153, 10.5 pgs.*

Pattern generator moves big-system resources onto designer's desktop. *Peters, Greg, Hewlett-Packard; Electronic Design, 09/19/85, pg 135, 7 pgs.*

Resistor gives timer a square-wave output. *Siegel, Andrew, Tufts; EDN, 07/11/85, pg 284, 1 pg.*

Timer chip drives high-voltage inverter. *Simonsen, Arnold N, Raytheon; EDN, 10/17/85, pg 170, 1 pg.*

V/F converter doubles output frequency. *Jung, Walt, Consultant; Travers, Don, Analog Devices; EDN, 10/31/85, pg 248, 1.33 pgs.*

Waveform generators take giant steps in precision and powers. *Johnson, Miller, Electronic Design, 06/06/85, pg 52, 3 pgs.*

Simulators/simulation

Input vectors drive simulation of logic-array designs. *Franz, Michael, Applied Micro Circuits; EDN, 06/13/85, pg 153, 6.75 pgs.*

Use simulation vectors to generate test vectors. *Franz, Michael, Applied Micro Circuits; EDN, 06/27/85, pg 233, 6 pgs.*

Sockets

IC-socket innovations keep pace with improvements in packaging technologies. *Leibson, Steve H, Southwestern Editor; EDN, 09/19/85, pg 61, 8.33 pgs.*

Speech synthesis/recognition

C program finds words that sound alike. *Grappel, Robert D, EDN, 07/11/85, pg 288, 1 pg.*

New algorithms, chips bestow human qualities on synthesized speech. *Bursky, Dave, Technology Editor; Electronic Design, 05/16/85, pg 113, 11.5 pgs.*

Philips's adapter box simplifies coding, editing. *Staff; Electronics, 06/10/85, pg 44, 4 pgs.*

Speech input system heeds data and commands with 1000-word recognition. *Goldhor, Richard, Kurzweil Applied Intelligence; Electronic Design, 06/27/85, pg 147, 6 pgs.*

Standards

AT&T's DMI integrates voice and data communications. *Mokhoff, Nicolas, Senior Editor; Computer Design, 09/01/85, pg 42, 2.5 pgs.*

Interchange format solves problems of design transfer. *LaBuda, Virgil P, Motorola; Waters, Michael, Motorola; Computer Design, 09/15/85, pg 103, 6 pgs.*

MAP standard gains VMEbus and Multibus I support. *Marrin, Ken, Senior Editor; Computer Design, 09/15/85, pg 49, 1 pg.*

Making the LAN connection with a fiber optic standard. *Joshi, Sunil P, Advanced Micro Devices; Computer Design, 09/01/85, pg 64, 6 pgs.*

Modern standards aimed at modern transmission schemes. *Repko, Marya, Bootstrap; Computer Design, 08/01/85, pg 119, 2.65 pgs.*

New IEEE-488 bus specs promise to ease systems integration and enhance performance. *Harold, Peter, European Editor; EDN, 09/19/85, pg 97, 6.66 pgs.*

Proprietary concerns may limit EDIF applications. *Goering, Richard, Field Editor; Computer Design, 08/01/85, pg 40, 1 pg.*

SCSI takes on additional I/O tasks. *Williams, Tom, West Coast Managing Editor; Computer Design, 09/15/85, pg 33, 1.5 pgs.*

Telecom chips: The new mass market. *Rosenberg, Robert, Communications Editor; Electronics, 09/30/85, pg 46, 5 pgs.*

Surface-mounting devices/techniques

PCB CAD systems tackle surface mount. *Goering, Richard, Field Editor; Computer Design, 07/15/85, pg 37, 3 pgs.*













Packaging changes make automatic testing tougher, more costly. *Bierman, Howard, Test & Measurement Editor; Electronics, 07/15/85, pg 48, 5 pgs.*

Specialized materials expand options in substrate design. *Dixon, Tom, Associate Editor; Electronic Products, 05/15/85, pg 59, 6 pgs.*

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Surface mounting shrinks resistor networks. *Chin, Spencer, Associate Editor; Electronic Products, 08/15/85, pg 51, 5 pgs.*

Surface-mounted components are not all alike. *Chin, Spencer, Associate Editor; Electronic Products, 10/15/85, pg 50, 7.5 pgs.*

Switches

Conductive elastomer vies for major switch role. *Byrbee, Crawford, Advanced Input Devices; Electronic Products, 07/15/85, pg 63, 3 pgs.*

Enhancements spurring electromechanical switches. *Chin, Spencer, Associate Editor; Electronic Products, 07/15/85, pg 47, 4.66 pgs.*

Membrane-switch choice is a joint design task. *DeGree, Dave, Bergquist Switch, et al; Electronic Products, 07/15/85, pg 57, 4 pgs.*

N+1 wires connect N Hall-effect switches. *Tacca, Hernán, Instituto de Ingeniería Biomédica; EDN, 07/11/85, pg 282, 1 pg.*

T

Tape drives

Cache memory splits computer and tape operations. *Thomas, Ron, Cipher Data Products; Computer Design, 10/01/85, pg 89, 4.5 pgs.*

Cartridge tape drives. *Wright, Maury, Western Editor; EDN, 10/31/85, pg 108, 12 pgs.*

PC-to-mainframe data link now a practical reality. *Killmon, Peg, Senior Editor; Computer Design, 08/15/85, pg 28, 1.5 pgs.*

Standards pave the way for tape cartridges. *Makmann, M Thomas, Archive; Computer Design, 05/85, pg 133, 5 pgs.*

Storage peripherals adapt to new demands for speed and capacity. *Killmon, Peg, Senior Editor; Computer Design, 05/85, pg 83, 10 pgs.*

Tape cartridge delivers hi-rel data. *Esboldt, Richard J, Memory Systems Lab; Electronic Products, 08/01/85, pg 55, 4.66 pgs.*

Two sides face off as ½-in. tape enters world of small computers. *Ohr, Stephan, Technology Editor; Electronic Design, 09/19/85, pg 57, 3.5 pgs.*

Technology/research, other

Slow and steady is the new strategy in automotive electronics. *Weber, David M, Industrial/Consumer Editor; Electronics, 06/17/85, pg 47, 6 pgs.*

Supercast ICs herald new supercomputer era. *Manuel, Tom, Computers & Peripherals Editor; Electronics, 09/09/85, pg 92, 5.5 pgs.*

VHSIC program moves on in Phase 2. *Myrvaaqnes, Rodney, Associate Editor; Electronic Products, 10/01/85, pg 45, 7 pgs.*

Telecommunications

AT&T's DMI integrates voice and data communications. *Mokhoff, Nicolas, Senior Editor; Computer Design, 09/01/85, pg 42, 2.5 pgs.*

Algorithms and chips cooperate to squeeze more speech signals into less bandwidth. *Bursky, Dave, Associate Managing Editor; Electronic Design, 10/03/85, pg 90, 9 pgs.*

Picture phone cuts time and cost in teleconferencing. *Staff; Electronics, 08/19/85, pg 34, 2.5 pgs.*

Understand FCC rules when designing telecomm equipment. *Dash, Glen, Dash, Straus, & Goodhue; EDN, 05/16/85, pg 193, 13.5 pgs.*

Temperature measurement

Current-source IC compensates for temperature errors. *Lee, Roland, Sensym; EDN, 10/03/85, pg 169, 4 pgs.*

Monitor thermocouples electronically. *Saberi, Marc, Masscomp; EDN, 10/17/85, pg 175, 1 pg.*

Thyristors

Gate-turn-off thyristors spec new current/voltage highs. *Harold, Peter, European Editor; EDN, 06/13/85, pg 61, 7.33 pgs.*

Timer ICs/circuits

Counter and PLA form µP watchdog timer. *Lett, David B, Scientific-Atlanta; EDN, 07/25/85, pg 310, 2 pgs.*

Simple techniques extend counter range. *Dattorro, Jon, Lexicon; EDN, 07/25/85, pg 307, 1 pg.*

Transmitter/receiver circuits

Circuit monitors RS-232C communications. *Griffin, Roy, M/A-Com; EDN, 08/08/85, pg 235, 1 pg.*

Design a simple dual-UART-based network. *Lowndes, Mike, Motorola; EDN, 06/13/85, pg 163, 6 pgs.*

Transceiver ICs adapt to use with all types of voice-data networks. *Mouton, Al, Motorola; Electronic Design, 07/11/85, pg 137, 5 pgs.*

U

Uninterruptible power supplies

Battery selection for UPS systems should be tailored to the application. *Massaro, Kevin, Gates Energy Products; Electronic Products, 06/03/85, pg 56, 5.66 pgs.*

Capacitor maintains data during power loss. *Crum, Stephen, Service Machine; EDN, 06/27/85, pg 241, 1 pg.*

Guidelines clarify backup needs in ups systems. *Massaro, Kevin, Gates Energy Products; Computer Design, 07/01/85, pg 129, 4 pgs.*

Switchers: Uninterruptible dc switchers. *Wright, Maury, Western Editor; EDN, 05/02/85, pg 139, 3.5 pgs.*

Uninterruptible supplies look to dc power. *Yates, Warren W, Associate Editor; Electronic Products, 05/15/85, pg 68, 5.33 pgs.*

Uninterruptible power supplies. *Butler, Robert, Electronic Design, 06/06/85, pg 181, 5 pgs.*

V

Video

Circuit clamps video signals. *Andelfinger, Richard, Hughes Aircraft; EDN, 05/16/85, pg 227, 1 pg.*

Computerized TVs use digital control and DSP techniques. *Harold, Peter, European Editor; EDN, 07/25/85, pg 195, 8 pgs.*

Vision systems

µCs handle image-processing tasks with help from boards and software. *Powers, Don, Contributing Editor; EDN, 06/20/85, pg 35, 9 pgs.*

Algorithms still key to computer vision systems. *Hindin, Harvey J, Special Features Editor; Computer Design, 05/85, pg 69, 4.33 pgs.*

Artificial intelligence the key to human-like vision systems. *Hindin, Harvey J, Special Features Editor; Computer Design, 06/85, pg 81, 3 pgs.*

Bigger bag of technology sharpens machine vision. *Weber, David M, Industrial & Consumer Editor; Electronics, 09/02/85, pg 41, 5 pgs.*

Character recognition and imaging come to the desktop. *Williams, Tom, West Coast Managing Editor; Computer Design, 08/01/85, pg 42, 2.5 pgs.*

Machine vision targets circuit errors automatically. *Dixon, Tom, Midwestern Editor; Electronic Products, 07/15/85, pg 34, 6 pgs.*

Video add-ons tap the IBM PC for inspection tasks. *Kenyon, Thomas, Windham Research; Preston, Craig, Data Translation; Electronic Products, 09/16/85, pg 82, 6 pgs.*

Voice-I/O equipment

DOD enlists voice control and expert systems. *Morgen, Bruce, Associate Editor; Electronic Products, 10/01/85, pg 65, 3 pgs.*

Market for speech ICs crumbles; software speech may fill the void. *Marrin, Ken, Senior Editor; Computer Design, 07/15/85, pg 19, 3.75 pgs.*

W

Waveform analyzers/analysis

Simple circuit suits quadrature detection. *Black, S L, AT&T Technologies; Maddox, H L, AT&T Technologies; EDN, 08/22/85, pg 203, 1 pg.*

Waveform synthesizer relies on equations to define complex signals. *Brodeur, Lester, Analogic; Electronic Design, 05/16/85, pg 155, 6.5 pgs.*

STANDARDS UPDATE

FCC EMISSION RULES — COMPUTERS, PERIPHERALS, AND ELECTRONIC EQUIPMENT, PART 15.

One million dollars in computer inventory was seized at Seequa Computer Corporation on July 24, 1985. U.S. Marshals made the seizure after the Federal Communications Commission found that Seequa's computers did not comply with FCC rules. The rules, under Part 15, require that virtually all electronic equipment, including computers, peripherals, and other digital hardware, comply with its emission limits. This seizure was the result of Seequa's having marketed equipment that emitted signals "in excess of that permitted by Commission regulations." The use of the seizure penalty of Title 47 of the U.S. Code, Section 508, is further evidence of the FCC's stepped-up enforcement campaign, which began with the creation of its Sampling and Measurement Branch one year ago and included at least two arrests and a record number of lesser penalties, such as fines and Public Notices.

Continuing tests for compliance are required under the FCC rules and regulations. In the Seequa case, the models seized had previously received FCC Certification. However, modifications were made and not reported to the FCC. Under a Public Notice issued April 7, 1982, the FCC requires manufacturers not only to have prototypes tested, but also to demonstrate continuing compliance as changes are made. Documentation must be kept on file, should the FCC's Field Operations Bureau call.

FCC compliance at a guaranteed rate by a guaranteed date is promised by Dash, Straus & Goodhue, Inc. (617-263-2662), the Northeast's largest research and development laboratory dedicated to EMI, ESD, and telecommunication research. From a detailed telephone conversation, engineers at DS&G can issue a fixed-price quote for having a device tested, modified where necessary, retested, and, if required, filed with FCC authorities. The combination of engineering and legal staff at DS&G will see you through the Commission's requirements in a minimum time. Dash, Straus & Goodhue's in-house legal staff will also assist clients, should the FCC call.

Two new policy papers have been released by employees of the FCC. While containing only their views as individuals, the papers are expected to have broad impact. One, by Richard Fabina, deals with test methods; the other, by Julius Knapp, deals with regulatory policy. Both are available free by calling DS&G at 617-263-2662.

FCC TELECOM RULES, PART 68.

"There is now evidence that telephone equipment can be fire hazards," announced the FCC in a notice to laboratories on June 28, 1985. The Consumer Product Safety Commission is investigating cases involving equipment which, while attached to a telephone line, caught fire. It appears that the use of Zener diodes as surge protectors may have been the cause. The failure mode was a short circuit, causing a one-half-watt, 20-ohm resistor to burn. The FCC also announced that as of September 1, 1985, no applications will be accepted without some explanation of how fire hazards were taken into account.

Compliance Design Inc. announces a new Part 68 Workstation™. The Workstation is designed for complete evaluations of telephones, modems, key systems, and PBXs for compliance with FCC, DOC, and EIA standards. Information on the Workstation has been filed with the FCC, and according to the company will soon be filed with Canada's Department of Communications. For further data, call Compliance Design at 617-264-4668.

Canada approves America. One year after the "Niagara Accords," in which Canada agreed to accept U.S. laboratories' data in its telecom certification program, the Department of Communications made good on its promise. However, only a few laboratories have met the DOC's comprehensive laboratory approval program, which includes on-site inspections, blind tests of sample telecom equipment, and detailed engineering briefs. Dash, Straus & Goodhue has become the Northeast's only Canadian-approved facility, and can now coordinate both U.S. and Canadian telecommunications approvals at significant savings in time and expense to its customers.

ELECTROSTATIC DISCHARGE.

The winter winds will bring colder temperatures and dryer air to the northern half of the country and, inevitably, a rise in computer crashes due to Electrostatic Discharge (ESD). Although line transients are often mistakenly suspected as the culprit, a simple spark from an operator's fingertip to a computer can cause loss of data or destruction of the system itself. As members of the American National Standards Institute's Working Group on Electrostatic Discharge, the engineers at Dash, Straus & Goodhue can test, modify, and verify equipment as complying with the latest U.S. and international standards.

The charge reservoir probe tip developed by Compliance Design (617-264-4668) is being studied by numerous companies as a basis for their in-house ESD standard. By placing a specially formed plate near the tip of the probe, the charge reservoir ESD simulator can achieve slew rates of 20,000 volts per nanosecond, as fast as any instrumentation in the world. Compliance Design can also supply information regarding which probe tips can be used to match the emerging U.S. and international standards.

WEST GERMAN REGULATIONS — VDE.

Like Canada, West Germany now recognizes U.S.-based test data, if the tests are properly performed and if the proper filings are made with West German authorities. Although the tests are similar to those required by the Federal Communications Commission, they differ in key areas such as radiated emissions below 30 MHz, an especially acute problem for CRTs.

A multinational staff located both in-house and through liaison contacts in West Germany has assisted DS&G's clients in meeting VDE requirements. DS&G can issue the "Gutachten" required for marketing equipment in Germany under its HfrG Law. The "Gutachten" will allow the equipment to be marketed anywhere in West Germany without filings by the user (i.e., "General Permit").

COMPLIANCE ENGINEERING 1985-1986, WILL SOON BE AVAILABLE.

Rapidly becoming the industry's standard handbook on EMI, ESD, and telecommunications compliance, *COMPLIANCE ENGINEERING* covers existing specifications and methods of engineering for compliance. Detailed appendixes on private and governmental contacts and FCC rules are included. The handbook is available free of charge by circling the last Reader Service Number below, or by calling Dash, Straus & Goodhue at 617-263-2662.

ANSI'S COMMITTEE ON OPEN AREA TEST SITES NEARS COMPLETION OF ITS WORK.

The group, which is setting standards for EMI test site construction will propose both a "Reference Site Method" and a "Reference Antenna Method" of calibration, the latter based on the Roberts™ Antenna developed by former FCC Lab Assistant Director Willmar Roberts. The antenna is available from Compliance Design at 617-264-4668.

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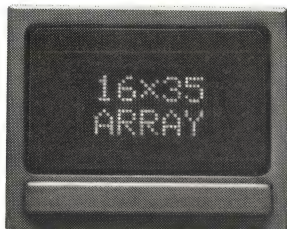
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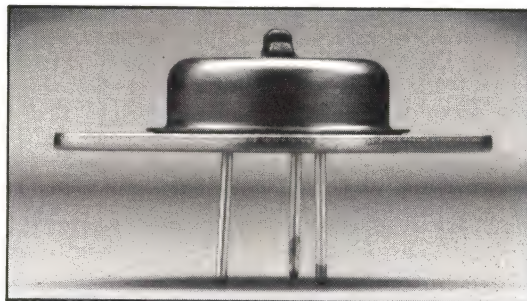
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1986

CALENDAR OF ELECTRONICS INDUSTRY EVENTS

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Motorola and Carroll Touch. Putting touch technology within reach.

When Carroll Touch, Inc. decided to redesign its line of touch input products, it had two major goals. One was to reduce the number of parts by 50 percent. Which meant Carroll Touch™ could drastically cut its manufacturing costs. And lower its price in the market.

The second goal was to build in an abundance of flexibility in a base product. This would allow Carroll Touch to expedite orders for custom systems. As well as respond to rapid changes in its market.

Carroll Touch achieved both of these goals when it unveiled its first model of the Smart-Frame™ scanning infrared touch input system. And the key ingredient was Motorola's MC68705R3 microcomputer.

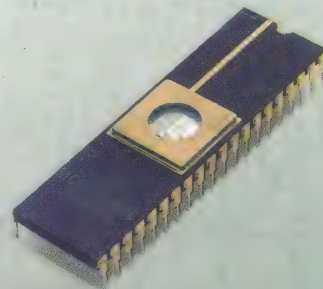
The MC68705R3 with its built-in EPROM gave the new Smart-Frame unprecedented flexibility. Special features could be added or changed by reprogramming Motorola's MCU instead of replacing it.

Because the MC68705R3 is a full-function microcomputer, most I/O support chips were eliminated. And many functions previously handled by task-specific hardware could now be handled by Motorola's MCU through software.

Motorola also satisfied the stringent requirements for reliability. Serviceability. And price. The MC68705R3 costs significantly less than its closest competitor. Yet its functionality and overall performance are significantly greater.

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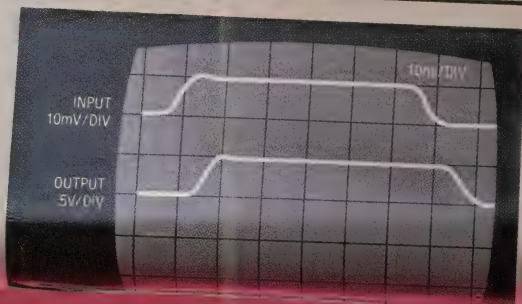
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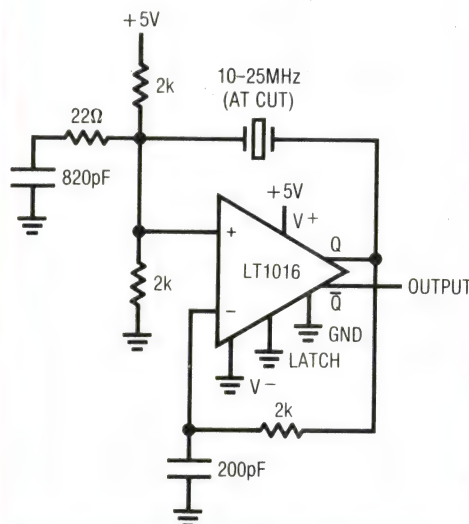


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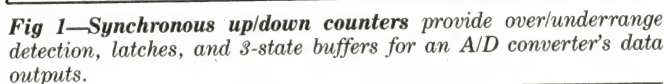
Robert J Inkol

The digital data outputs of many A/D converters lack sufficient current drive to handle the capacitance associated with heavily loaded buses. In addition, for systems that perform further digital processing, you might need to detect digital-overrange conditions. The **Fig 1** circuit stores a converter's outputs in a clocked register, provides 3-state buffers, and detects either extreme of the binary range.

The circuit implements these three functions with synchronous binary up/down counters (such as 74ALS569s), which latch the A/D-converter outputs on positive clock transitions. The counters' clocked carry outputs (CCO) go low when the data outputs are enabled and the clock signal is low. Accordingly, IC₁'s CCO signal can serve as an asynchronous system reset, or it can trigger a monostable multivibrator that drives an LED to provide a visual overrange warning. The CCO signal is internally gated with the clock signal to eliminate the decoding glitches commonly associated with a ripple-carry output.

An up/down counter lets you detect both ends of the converter's output range—ie, all zeros as well as all ones. (You can detect both ends of the converter's output range for BCD data by using a 74ALS568 BCD counter.) The OVERRANGE output in **Fig 1** is disabled when OUTPUT ENABLE goes high, thereby placing the data outputs in the high-impedance state. If you don't require 3-state outputs, you can obtain eight data bits per IC using 74AS869 up/down counters. (Note, however, the 74AS869's CCO is not internally gated with the clock. To avoid decoding glitches, you must provide an external gate or connect the first counter's ENT input to the clock.)

The speed of this circuit depends on the number and the type of ICs you use. For 12-bit data, you can achieve 10-MHz operation with 74ALS logic; you can achieve 20-MHz operation with 74AS logic. **EDN**

EDN

Product detection simplifies HF receiver

Shlomo Varsano

Southern California Edison, Alhambra, CA

The 3- to 30-MHz high-frequency (HF) band, used primarily for long-range communications, also serves as a backup link for other frequency bands that sometimes become crowded and require the use of a high-selectivity receiver. Using a product detector (Fig 1), you can build a high-selectivity receiver and avoid the expense of a more complex design based on a synchronous oscillator. One advantage of product detection over the alternative envelope-detection scheme is a reduction in the selective fading that occurs as the incoming signal's carrier amplitude varies with respect to the sideband amplitudes.

AM detection is accomplished in the Fig 2 limiter/multiplier circuit, which is based on a dual differential-amplifier transistor array. The IF signal (which should be less than 0.5V p-p) is capacitively coupled to the differential amplifier formed by transistors Q_3 and Q_6 . At the same time, an amplified version of the IF signal

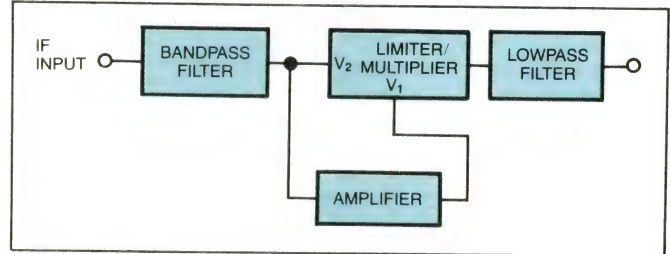


Fig 1—Based on a product detector, this AM synchronous demodulator simplifies HF-receiver design.

is coupled to the bases of Q_1 and Q_5 . The four upper transistors serve as switches, connecting alternate half cycles of the IF (V_2) signal to opposite sides of the differential amplifier. The result is a multiplication of the V_1 and V_2 inputs, yielding full-wave rectification of the IF signal. Q_7 and Q_8 form a constant-current source to provide constant transconductance in the differential amplifier.

The 2.4-k Ω value of the emitter resistors for transistors Q_3 and Q_6 ensures that the transistors' collector-current nonlinearity is less than 1%. Further, to

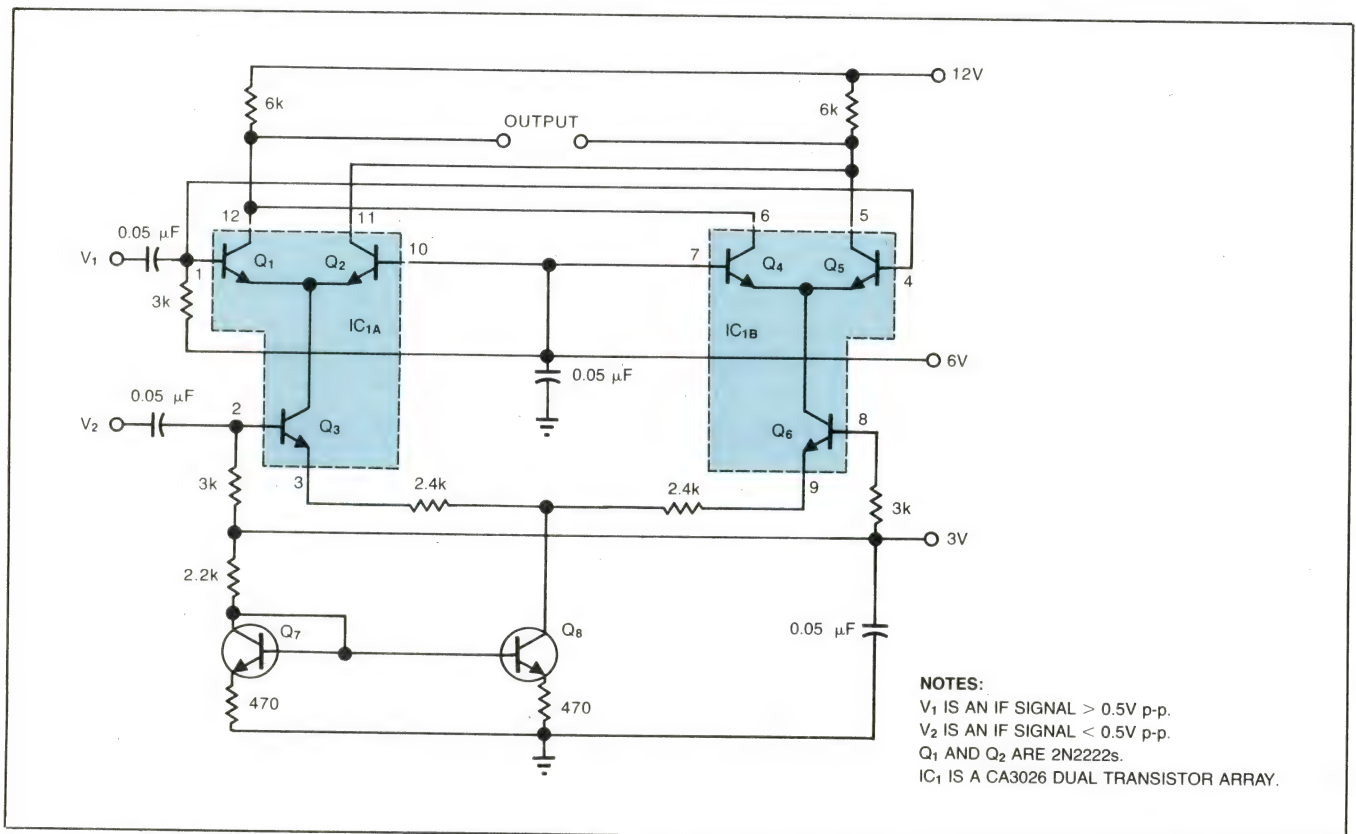
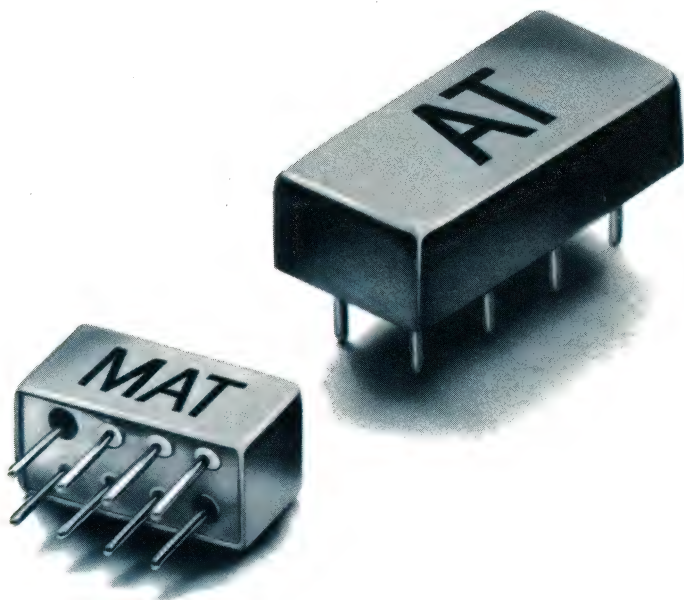


Fig 2—This multiplier/limiter circuit multiplies the IF carrier (V_1) by the sideband information (V_2) to produce full-wave rectification of the IF signal.

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DESIGN IDEAS

achieve 1% or less second-harmonic distortion (for a 30% modulation ratio), the ratio of sideband to carrier amplitude at the multiplier's input must be less than 0.043. You can meet the sideband-to-carrier-amplitude ratio requirement via amplification and limiting within the switching stages (Q_1 - Q_2 and Q_4 - Q_5), thus ensuring that the carrier amplitude (produced by V_1) is much greater than the sideband amplitudes (obtained from V_2).

EDN

Reference

1. *Transmission Systems for Communications*, Bell Telephone Laboratories Inc, Holmdel, NJ, 1971.

To Vote For This Design, Circle No 431

Biquad filter offers adjustable f_0 and Q

Prabhas Gangopadhyay
Hagersten, Sweden

A switched-capacitor bandpass filter (Fig 1) gives you independent control of output center frequency (f_0) and selectivity (Q). The LF356 op amps used in the circuit are well suited to this application because they remain stable while driving capacitive loads as high as $0.01 \mu\text{F}$. Each switch uses half of a CD4016 quad bilateral switch

IC, driven by nonoverlapping clock signals CLK_1 and CLK_2 from the clock generator (Fig 2).

Use the following relationships to calculate the values for C_1 , C_5 , C_6 , and C_7 , based on a value of 1 for capacitors C_2 , C_3 , and C_4 :

$$C_1 = 2Q$$

$$C_5 = 2 \tan(\pi f_0 / f_s)$$

$$C_6 = C_7 = \sin(2\pi f_0 / f_s),$$

where f_s is the frequency of the nonoverlapping clock

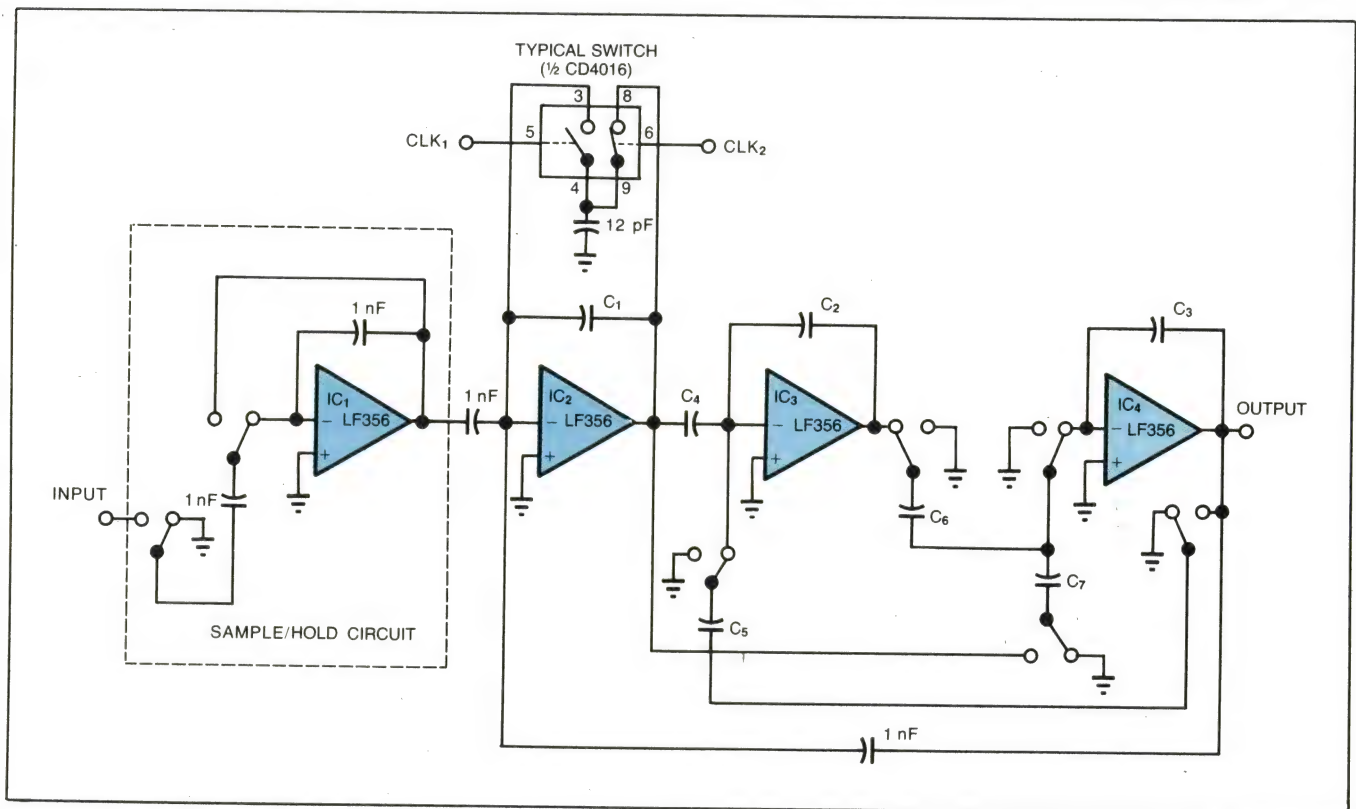


Fig 1—Four op amps and four quad-switch ICs make up a switched-capacitor bandpass filter with independent control of center frequency and Q .

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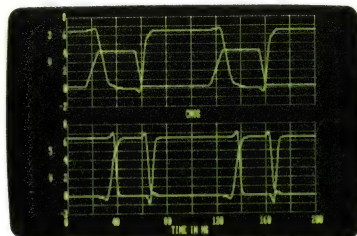
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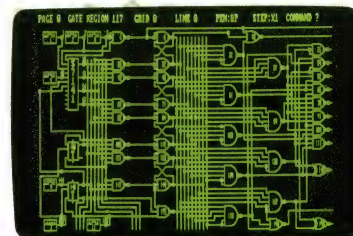


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works. In addition, you get even more advanced device models, worst case capabilities, temperature stepping, Fourier analysis, and macro capability.

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MICROLOGIC provides you with a similar interactive drawing and analysis environment for digital work. Using standard PC hardware, you can create logic diagrams of up to 9 pages with each containing up to 200 gates. The system automatically creates the netlist required for a timing simulation and will handle networks of up to 1800 gates. It provides you with libraries for 36 user-defined basic gate types, 36 data channels of 256 bits each, 10 user-defined clock waveforms, and up to 50 macros in each network. MICROLOGIC produces high-resolution timing diagrams showing selected waveforms and associated delays, glitches, and spikes—just like the real thing.



"Typical MICROLOGIC Diagram"

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Regarding MICROCAP... "A highly recommended analog design program" (PC Tech Journal 3/84). "A valuable tool for circuit designers" (Personal Software Magazine 11/83).

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MICROCAP and MICROLOGIC are available for the Apple II (64k), IBM PC (128k), and HP-150 computers and priced at \$475 and \$450 respectively. Demo versions are available for \$75.

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DESIGN IDEAS

signals and $f_0 < f_s/2$. The gain of this filter at f_0 is 0 dB.

You can set Q by adjusting the C_1 value. In addition, values for C_5 and C_6 determine the $f_0:f_s$ ratio, allowing you to control f_0 by adjusting the clock frequency.

For example, assume $f_s=64$ kHz, and you require $Q=2$ and $f_0=10$ kHz. The equations yield $C_1=4$, $C_5=1.0690$, and both C_6 and $C_7=0.8315$. You might scale these values by a convenient constant, such as 2.8, and obtain $C_1=4$ nF, $C_2=C_3=C_4=2.8$ nF, $C_5=2.9932$ nF, and

C_6 and $C_7=2.3282$ nF.

IC₂'s inverting input requires a dc path to ground for input bias currents; the dc path is supplied by the 12-pF switched capacitor. The filter performs well with $\pm 5V$ supplies.

EDN

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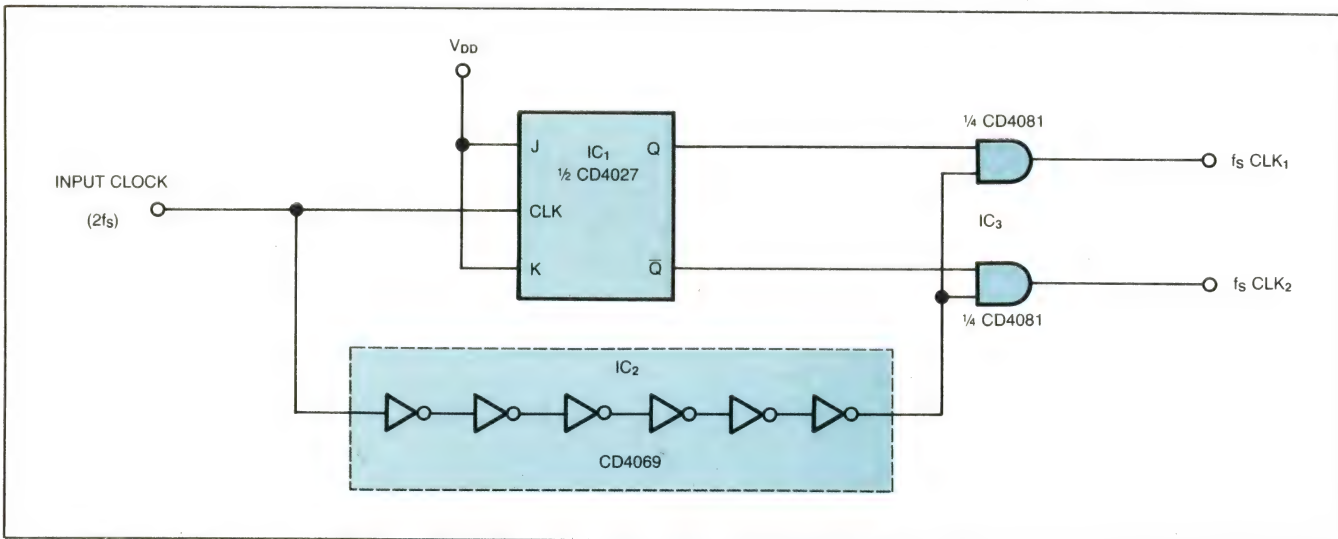


Fig 2—Using three ICs, you can generate nonoverlapping clock signals to drive the switches of the circuit in Fig 1.

68020 adapter upgrades 68000 systems

Brian Koga
Wang Laboratories Inc, Lowell, MA

By using a plug-in adapter board (Fig 1, pg 218), you can replace a 16-bit 68000 CPU with the 32-bit 68020 CPU, which offers a larger instruction set and faster program execution. The resulting system requires some modification of operating-system software but no additional hardware changes.

The adapter board plugs into the 68000 socket as an emulator does. Because the 68020 can operate on a 16-bit data bus as well as a 32-bit data bus, wiring modifications consist only of connecting D_0 through D_{15} of the 68000 to D_{16} through D_{31} of the 68020 data bus. All other address (A_1 through A_{23}) and control signals with corresponding names are wired one for one; address lines A_{24} through A_{31} are unconnected.

The 68020 requires six additional signals: AVEC, E,

VMA, LDS, UDS, and DSACK₁. AVEC, E, VMA, and DSACK₁ are generated with proper timing relationships by logic gates on the adapter board. LDS and UDS are generated by decoding the SIZ₀, SIZ₁, and A_0 signals and qualifying them with DS.

Keep in mind that the two processors handle exception processing differently. The 68020 stacks as many as 46 words during exception processing, but the 68000 stacks only three words. In the worst case, the CPU will halt if software doesn't compensate for this difference. Also, the 68020 generates the address strobe (AS) on the clock's falling edge (state 1), but the 68000 generates AS on the rising edge (state 2). If your hardware timing relies on the latter, you must invert the clock signal (CPUCLK) to the 68020.

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CIRCLE NO 139

**Mepco/Electra Film Capacitor
Typical Characteristics**

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Operating Temp. °C	-55°C to +125°C	-55°C to +125°C	-55°C to +105°C	-55°C to +70°C (85°C)
Dissipation Factor % 1KHz 25°C	1.0% MAX	3% MAX	.1% MAX	.1% MAX
Dielectric Constant (Practical)	3.1	3.0	2.2	2.5
% Capacitance Change (Temp. Range)	-6% to +16%	±2% Over Temp.	±2% Over Temp.	-120 to ±60 PPM/°C
Relative Cost	Low	Med.	Med.	High
Cautions	None	Humid	Temp.	Temp.

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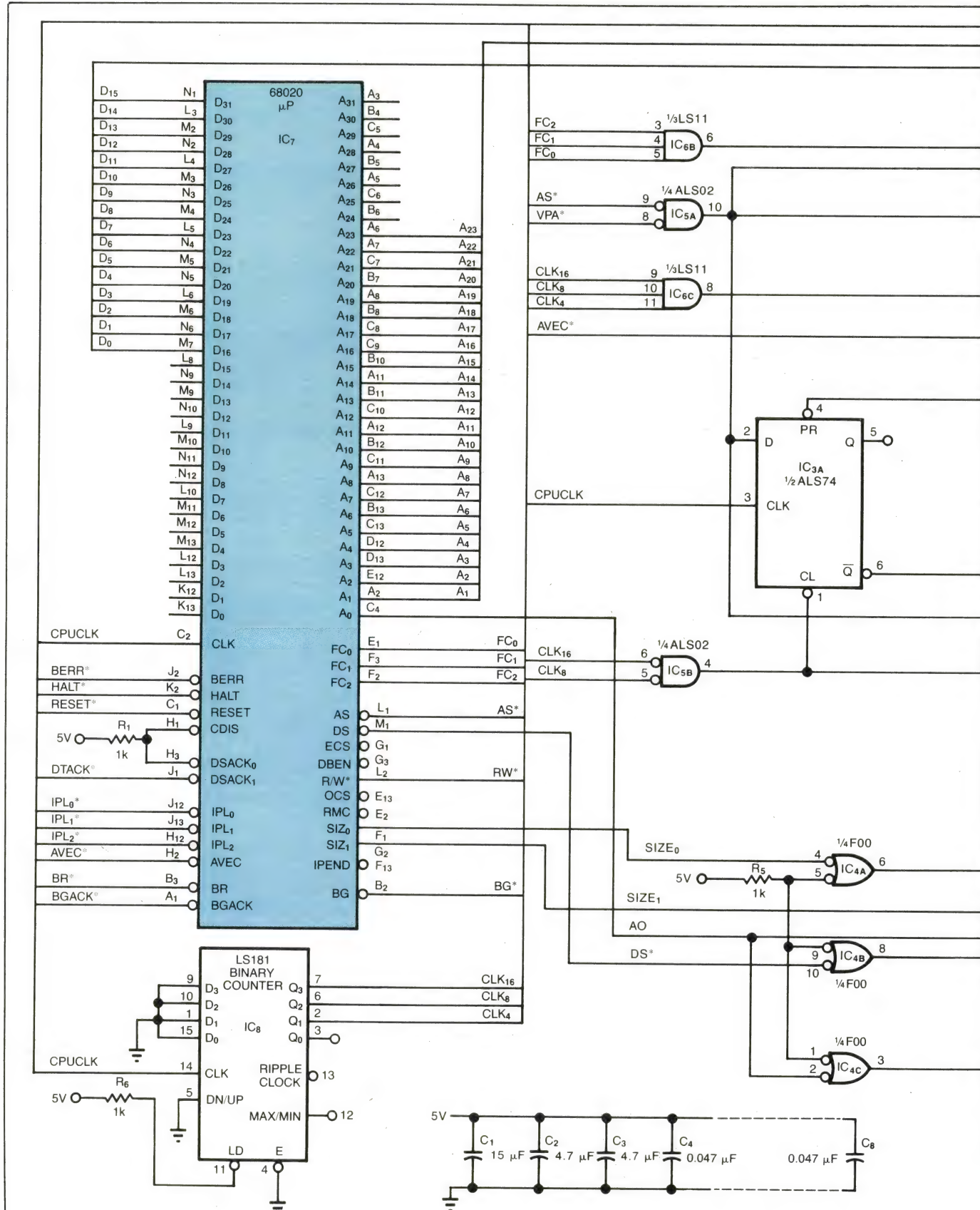


Fig 1—This 68020 adapter board plugs into a 68000 socket to provide the benefits of the more powerful 32-bit processor.

DESIGN IDEAS



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Use SWI instruction for 6805 Push operation

Larry D Iffrig
AT&T Technologies Inc, Ballwin, MO

Unlike the 8085 microprocessor, the 6805 μ P has no Push and Pop instructions. You can, however, gain access to the contents of the accumulator, index, and condition-code registers and perform operations on them.

To do so, first write an appropriate vector address to the software-interrupt (SWI) location FFC_{HEX}/FFD_{HEX} . Place a return-from-interrupt (RTI) instruction at the location indicated by that address.

Next, place an SWI instruction at the point in your program where you want to copy and save the accumulator, index, and condition-code register contents. These contents are automatically pushed onto the stack as part of the SWI operation. From this point in your program, calls to subroutines (BSR and JSR operations) will affect the program-counter contents only at this saved location within the stack.

You can now use register-direct instructions to perform operations based on the contents of these saved registers. Suppose, for example, that the stack pointer is set at $07F_{HEX}$ (reset address); suppose also that your program is to perform a compare operation and that you want to execute a branch-if-equal (BEQ) function later in the program. If the compare result is equal, bit 1 in the condition-code register will be set. An SWI instruction following the compare operation will then save the condition code at stack location $07B_{HEX}$. You can later test the bit using "BRSET 1, \$07B" to make the required branch.

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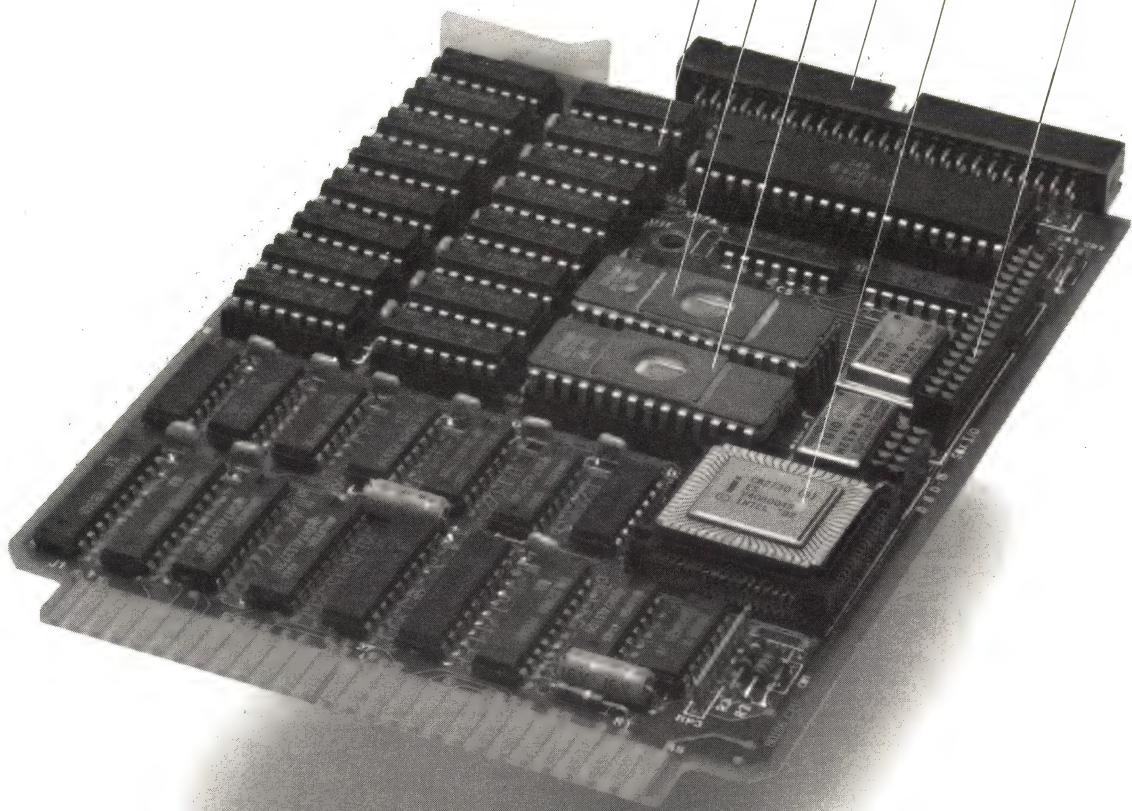
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PC-BOARD LAYOUT

This CAD system for pc-board layout, Board Designer, consists of a Scaldsystem workstation and a MicroVAX II-based pc-board router, ValidRoute. Secmai (Alfortville, France) developed this router. The MicroVAX II functions as a server for pc-board design, which you can access via Ethernet or DECnet. The design system provides interactive, semiautomatic, and fully automatic pc-board placement and routing. The automatic mode includes iterative or automatic placement improvement with gate and pin swapping. Semiautomatic routing offers net-routing and point-routing algorithms. The CAD system is re-entrant, which means that you can switch among interactive, semiautomatic, and automatic modes. The layout package handles as many as 16 signal layers; it generates fabrication and assembly drawings, tapes to control photoplotters, and tapes that drive numerically controlled drilling machines. Board Designer and workstation, \$120,000; MicroVax II server and ValidRoute software alone, \$75,000.

Valid Logic Systems Inc., 2820 Orchard Parkway, San Jose, CA 95134. Phone (408) 945-9400. TLX 3719004.

Circle No 350

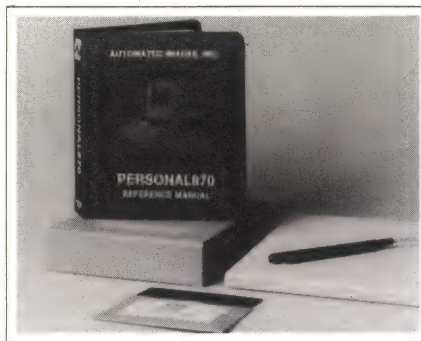
COLOR WORKSTATIONS

The CDX-9300S, CDX-5900S, CDX-50000S, and CDX-59000S workstations all offer performance improvements over their respective predecessors, according to the manufacturer. All four workstations use either a 12.5-MHz or a 16-MHz

68020 μ P. In addition, the memory-management unit of each can handle as much as 12M bytes; standard memory configurations contain 4M bytes. The CDX-9300S and 5900S have software that includes Unix, a C compiler, custom postprocessing of files, a hierarchical schematic editor, a virtual logic analyzer, and the Cadat logic simulator. The CDX-5900S differs from the CDX-9300S because the 5900S provides automatic pc-board placement and routing as well as manufacturing postprocessors. CDX-59000S, \$96,900; CDX-50000S, \$82,900; CDX-5900S, \$71,400; CDX-9300S, \$59,000. Delivery, 30 to 60 days ARO.

Cadnetix Corp., 5757 Central Ave, Boulder, CO 80301. Phone (303) 444-8075.

Circle No 351

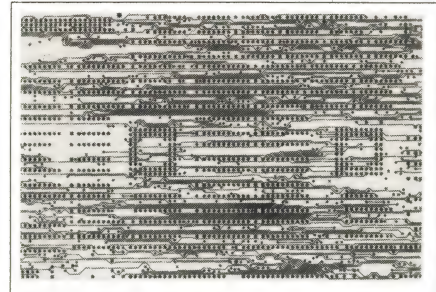


PC-BOARD DESIGN

Running on an IBM PC/XT, PC/AT, or compatible personal computer, Personal870 designs and lays out pc boards. It can work alone or interface to the Applicon Graphics System 870. The package is compatible with the FutureNet database. You can also interface the schematic editor to Automated Systems Inc's mainframe-based France layout system. After completing a pc-board layout, you can transfer PC-based schematics to your design system and back annotate your design. \$8000.

Automated Images Inc., 53 Cummings Park, Woburn MA 01801. Phone (617) 933-1731.

Circle No 352



PC-BOARD CAD

Dash-PCB, developed by Vectron Graphics (Santa Clara, CA) for VAX-class processors, now runs on an IBM PC equipped with a 32-bit coprocessor board. The system designs and lays out pc boards directly from Dash schematic-design net lists. The system uses as many as five different routing algorithms, each of which attempts to maximize board density. You must place components interactively. The display shows the origins and destinations of all interconnections. As you move parts on your screen, all the nets that you have selected stretch and contract. An automatic 2-step routing process sequences through a predetermined (or default) mix of routing algorithms. The first stage of each algorithm is a macrorouter that examines 1-in.-wide paths of board space to see if the route can be taken without any feedthroughs. Each algorithm's second stage is a microrouter that routes a matrix as fine as 1-mil points in a 1-in.-wide path. Additional software facilities provide six postprocessing tasks: back annotation, automatic parts-insertion tapes, bill of materials and parts, numerically controlled drill tapes, fabrication drawings, and assembly drawings. \$13,000.

FutureNet Corp., 9310 Topanga Canyon Blvd, Chatsworth, CA 91311. Phone (818) 700-0691. TWX 910-494-2681.

Circle No 353

ANALOG MODELING

ChipSim, DPAX, AdLib, and the Analog Libraries are all part of this company's Analog Design Series.

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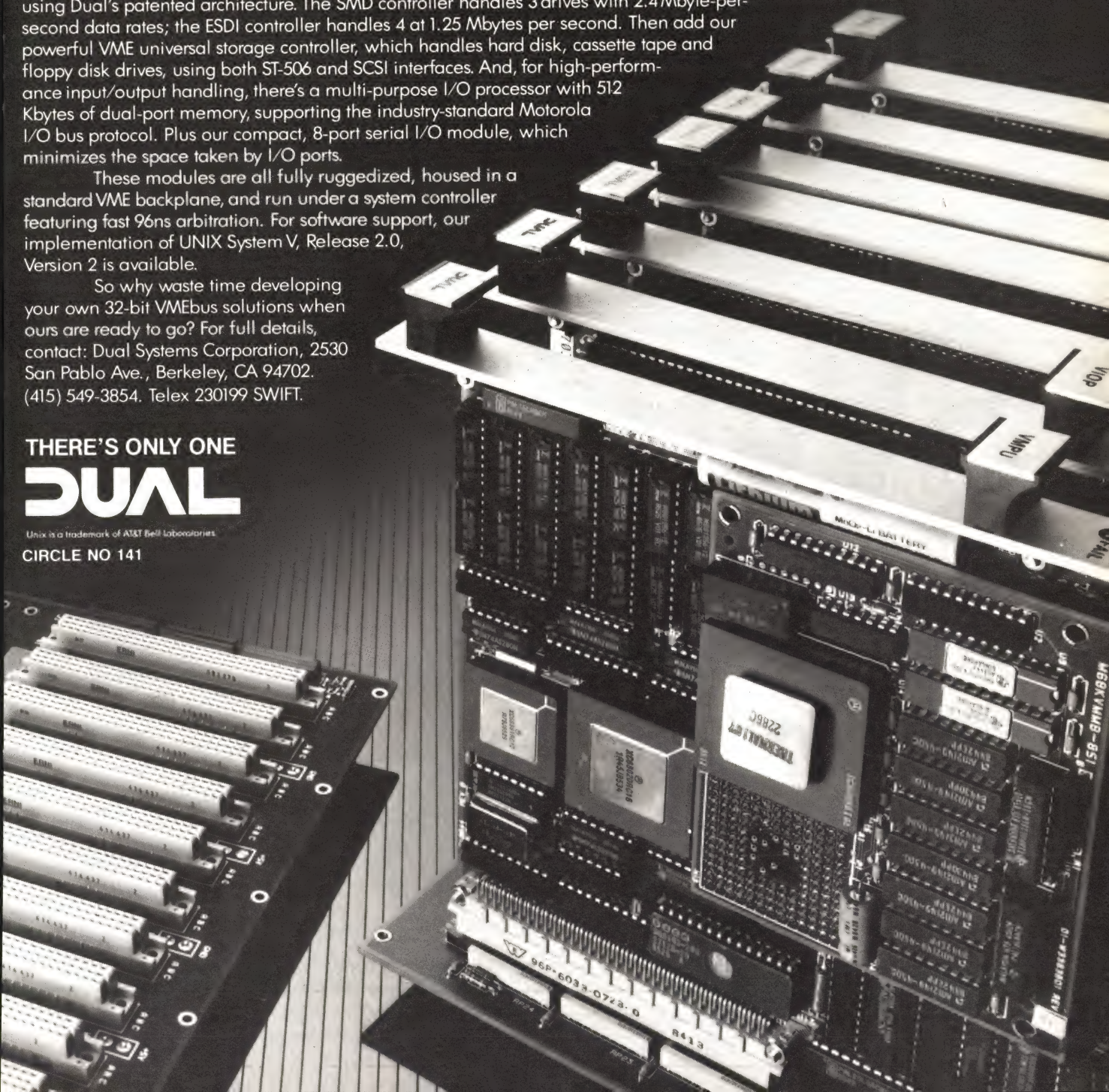
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Daisy Systems Corp., 700 Middlefield Rd, Mountain View, CA 94043.
Phone (415) 960-0123.

Circle No 354

STANDARD-CELL CAD

A 2- μ m CMOS library of more than 250 standard cells runs on VAX, MicroVAX, Ridge, Apollo, Elxsi, and HP 9000 computers. The library includes schematic icons and simulation models of 250 digital cells; a library of this company's Megacells for highly integrated μ Ps; and silicon compilers for functions such as RAMs, ROMs, and PLAs. The package also provides IC-design tools such as automatic placement and routing. The vendor offers prototyping and manufacturing services for the 2- μ m double-metal CMOS process. The digital-cell library contains gates, flip-flops, multiplexers, counters, and I/O pads. \$5000/license.

VLSI Technology Inc., 1109 McKay Dr, San Jose, CA 95131.
Phone (408) 942-1810.

Circle No 355

PC/MICROVAX CAE

The CT4000 CAE package runs on the MicroVAX II and the VAXstation II supermicrocomputers.

EDN January 9, 1986



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		Low cost personal computer	Business use computer		CAD/CAM graphic terminal		
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	Stripe	A22JCM00X (0.47mm)	—	—	—	—	—
11V	Dot	—	M29JAW00X (0.38mm)	M29JNA00X (0.28mm) M29JCA50X (0.31mm)	M29JCQ11X* (0.21mm)	—	—
13V	Dot	—	M34JMA03X (0.39mm) M34JAW03X (0.43mm)	M34JCA03X (0.31mm)	M34JKS02X (0.26mm)	M34JFM22X (0.21mm)	—
	Stripe	M34JDV13X (0.51mm)	M34JBK11X (0.41mm)	—	—	—	—
14V FS	Dot	—	—	—	M36JCA00X (0.28mm)	—	—
	Stripe	A36JFT00X (0.51mm)	M36JJQ00X (0.42mm)	—	—	—	—
19V	Dot	—	—	510ABTB22 (0.47mm)	M48JLK22X (0.31mm)	M48JKT22X* (0.26mm)	M48JMG21X* (0.21mm)

* Under development () : Phosphor triplet pitch



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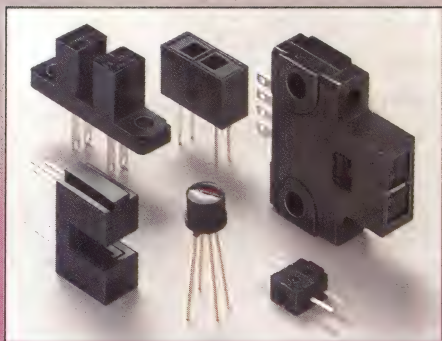
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The package uses the same command set as the IBM PC-compatible version. You can pass graphical and hierarchical files between PCs and MicroVAX II computers. The package includes a graphics editor, pc-board layout tools, the Scald hardware compiler, net-list post-processor, timing verifier, and logic simulator. \$11,900.

Case Technology Inc., 633 Menlo Ave, Suite 250, Menlo Park, CA 94025. Phone (415) 322-4057.

Circle No 356

LOGIC ACCELERATOR

The Eventlink option opens the architecture of this company's Logic Evaluator and Expeditor logic-simulation accelerators, which allows the simulation packages to interactively exchange data with other CAE systems. Features include an interface to physical-modeling devices; an interactive event interface, which allows concurrent operation with any other application that generates or uses events; and a dual system interface, which lets two host systems share a single hardware accelerator. Sample-time processing control sets the hardware accelerator so it stops at specified sample times and waits for instructions. A Breakpoint control terminates simulations upon reaching a trigger event. EventLink option on the Logic Evaluator, \$20,000; on the Expeditor, \$12,500.

Zycad Corp., 3499 Lexington Ave N, St Paul, MN 55112. Phone (612) 631-3175. TLX 291040.

Circle No 357

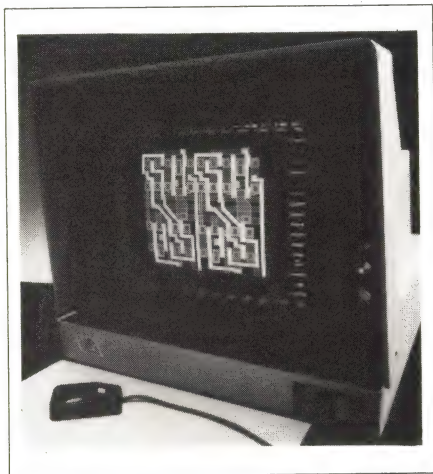
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Personal CAD Systems Inc., 981 University Ave, Bldg B, Los Gatos, CA 95030. Phone (408) 354-7193. TLX 278866.

Circle No 358



SEMICUSTOM-IC CAD

This processing - technology - independent package, BuildingBlocks, is a hierarchical automatic placement and routing package. The package uses a library of predefined functional blocks that can be as complex as a μ P or as simple as a transistor. The blocks in the library can be irregular in shape; you can draw them by hand or direct the package to generate them automatically.

The package combines chip-level placement, routing, editing, and analysis with cell-level physical design and editing. ChipTool-II, a cell editor and block generator, is an option for the design package that generates artwork (such as logos). Other options are GenLib 3000, a standard-cell library that features both single-layer- and double-layer-metal cells, and PG-Tool, which produces tapes for optical and electron-beam pattern generation. BuildingBlocks, \$55,000; ChipTool, \$20,000; GenLib, from \$5000; PG-Tool, from \$10,000. Delivery, 60 days ARO.

Via Systems Inc., 76 Treble Cove Rd, North Billerica, MA 01862. Phone (617) 667-8574.

Circle No 359

IC-MODULE DESIGN

The Genesis silicon development system is a set of tools for VLSI-IC design. It develops function compilers that can implement IC functions like EEPROMs, multipliers, and register files. The tools synthesize layout, timing, function, and power modules, as well as schematics. The system provides layout-vs-schematic checking, electrical- and design-rules checking, logical design-rules checking, Spice deck verification, circuit analysis, and timing verification. The package also interfaces to test instruments. IC-design tools include an automatic router, a package editor, and pattern generation. Genecal, a second set of tools, works with both Genesis and the company's Genesil design system; it enables IC manufacturers to specify their own processing technology. Owners of Genesil can add Genesis for \$30,000; complete turnkey Genesis system, from \$95,000; Genecal, \$45,000.

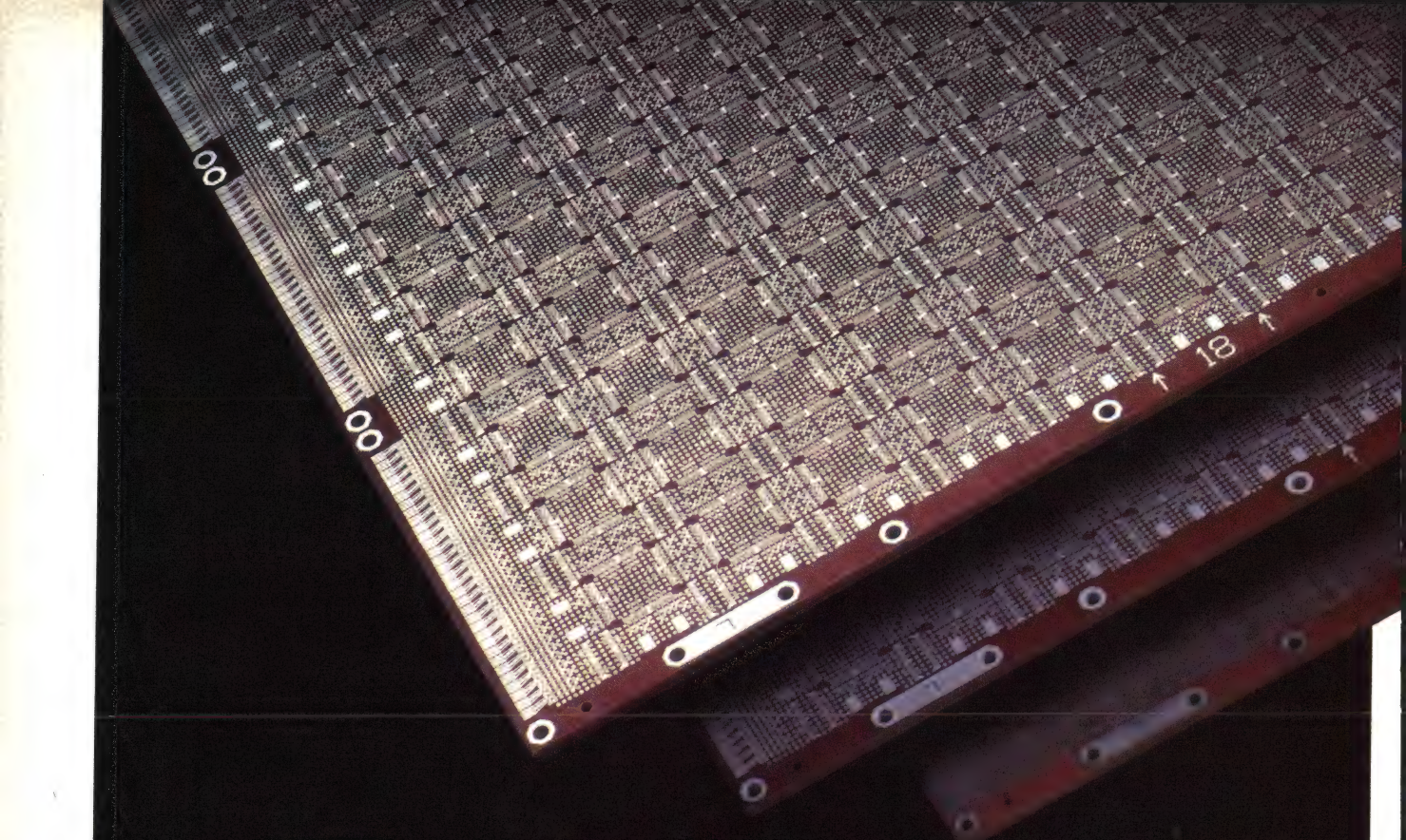
Silicon Compilers Inc., 2045 Hamilton Ave, San Jose, CA 95125. Phone (408) 371-2900.

Circle No 360



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CIRCLE NO 234



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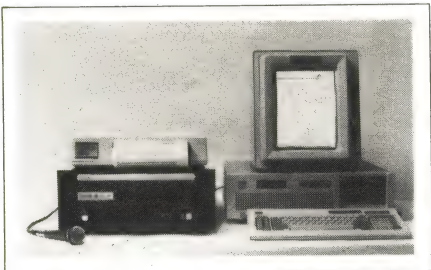
Phone _____

Mail to: Fujitsu America, Inc., Data
Products Division, 3055 Orchard Dr.
San Jose, CA 95134

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3055 ORCHARD DRIVE
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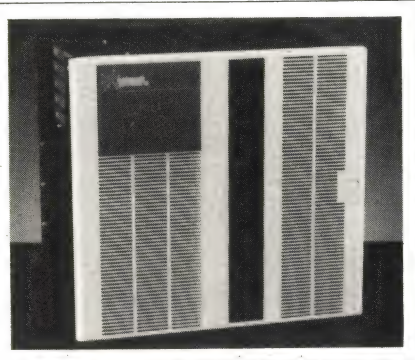


OPTICAL DISK

Providing storage for as much as 3G bytes of text data or 50G bytes of image data, the Discus 1000 optical-disk subsystem for IBM PCs and compatibles gives you write-once, read-many data storage in a desktop unit. The 12-in. removable optical disk has an on-line data-storage capacity of 1G byte; however, you can order an optional text-, image-, and sound-compression function to expand the unit's total storage capacity to a maximum of 50G bytes—roughly equivalent to two million pages of data, 50,000 8.5×11-in. images, or 30,000 hours of audio. You can mix text and graphics in the recording process. The subsystem includes a laser and optical head for permanent data recording and gives you random or sequential access to data records. From \$21,500.

AGA Inc., 347 Fifth Ave, New York, NY 10016. Phone (212) 683-9160.

Circle No 361

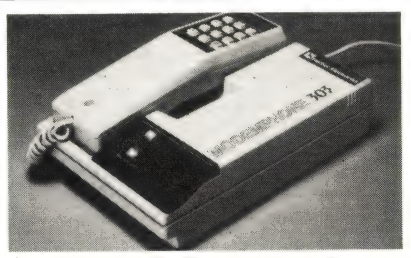


DATA PBX

The Virtual Circuit Exchange (VCX), initially introduced as a simple data PBX for limited local-area data exchange, is expandable into a high-speed network with local, national, or international transmission paths. The VCX system provides this upgrade via V.11 and V.35 interfaces that can operate with transmission media such as twisted-pair cables, short-haul modems, microwave links, fiber-optic links, and T1 subchannels. The key to the VCX's expansion capabilities is its intelligent virtual connections. Each V.11 or V.35 line card supports two trunks; you can house as many as 19 line cards in one chassis. \$2500 per line card.

Network Products Inc., Research Triangle Park, NC 27709. Phone (919) 544-8080. TLX 802855.

Circle No 362



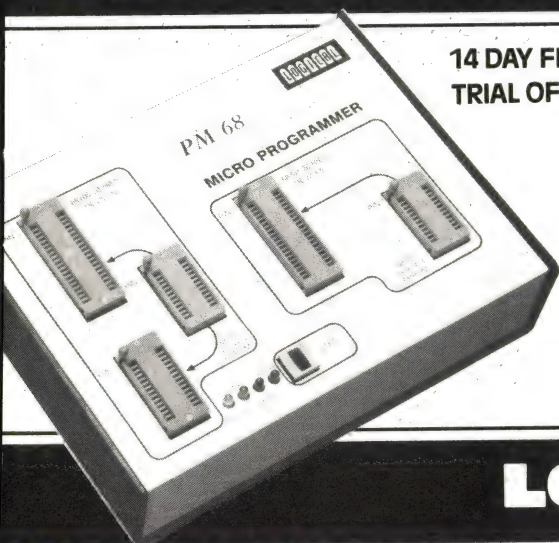
MODEM PHONE

The Modemphone 303 is both a 300-bps modem and a telephone. The modem features automatic or manual answering, manual call origination, and automatic disconnection. You can connect it to an Apple, IBM PC, or compatible computer via an RS-232C interface. Communications software is included. For conversations, you can either use the telephone's receiver or convert the unit into a speakerphone for hands-free operation. Other phone features include a pushbutton keyboard that works with pulse and tone lines, an "in-use" dialing indicator, last-number redial, autodialing with a 10-number memory, and a 12V ac power adapter. The Modemphone 303 plugs into standard RJ11 modular jacks. \$149.

Harbor Electronics, 650 Danbury Rd, Ridgefield, CT 06877. Phone (800) 243-4794; in CT, (203) 438-9625.

Circle No 363

SINGLE-CHIP MICRO PROGRAMMERS: UNDER \$500



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The stand-alone PM 68 or PROMPRO-7 Micro Programmer is a self-contained unit designed for production and engineering.

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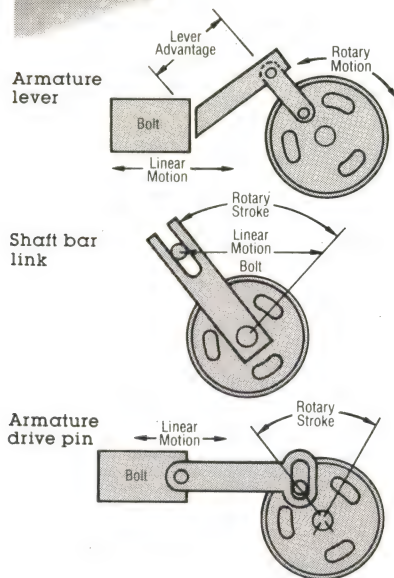
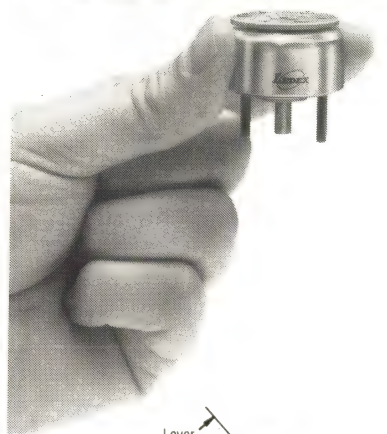
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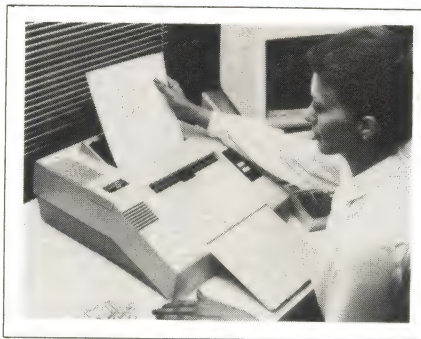
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COMPUTERS & PERIPHERALS



PAGE READERS

The PCS 230 and PCS 240 desktop scanners permit IBM PCs (or compatible systems) to enter text without manual rekeying. The PCS 240 also adds image scanning, thus allowing your PC to store both text and graphics. These optical-character-recognition devices can read and recognize a standard 8½×11-in. page of text in approximately 30 sec or a page of graphics in 12 sec. Recognition algorithms let the units identify various typestyles (eg, Courier 10 and 12, Titan 10 and 12, Letter Gothic, elite, and pica). The scanners can even handle proportionally spaced, right-justified text and special symbols. The PCS 240 enters graphics in the form of bit-mapped images. This model also gives you the ability to manipulate images, annotate an image with comments or legends, or produce composite text/graphic documents. Both models perform unattended scanning. The units have only two control buttons; the load trays accept as many as 50 sheets of paper in mixed sizes and weights. PCS 230, \$5695; 240, \$5995.

Compuscan Inc., 81 Two Bridges Rd, Bldg 2, Fairfield, NJ 07006. Phone (201) 575-0500. TLX 219267.

Circle No 364

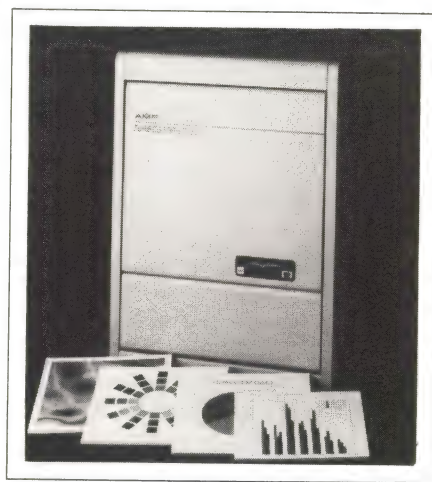
LASER PRINTER

The Opus 1 laser printer suits letter-quality printing workloads of 20,000 pages/month in a multiple-user environment. Print resolution is 300×300 dots/in.² and print speed is 12 pgs/minute. It offers three operating modes: setup, type, and

draw. The setup mode lets you customize fonts by changing the height, width, or grade slant on one of four basic fonts stored in the printer. You can also mix font sets throughout a document and store logotypes. It allows you to store forms for as many as four document formats such as reports or invoices. The type mode lets the printer emulate Diablo and Qume daisy-wheel printers. The draw mode provides you with limited linear graphic capability in eight directions and five line widths. The Opus 1 includes a parallel and a serial interface. Its paper tray holds 250 sheets of paper. \$9500.

Facit Inc., 9 Executive Dr, Merrimack, NH 03054. Phone (603) 424-8000.

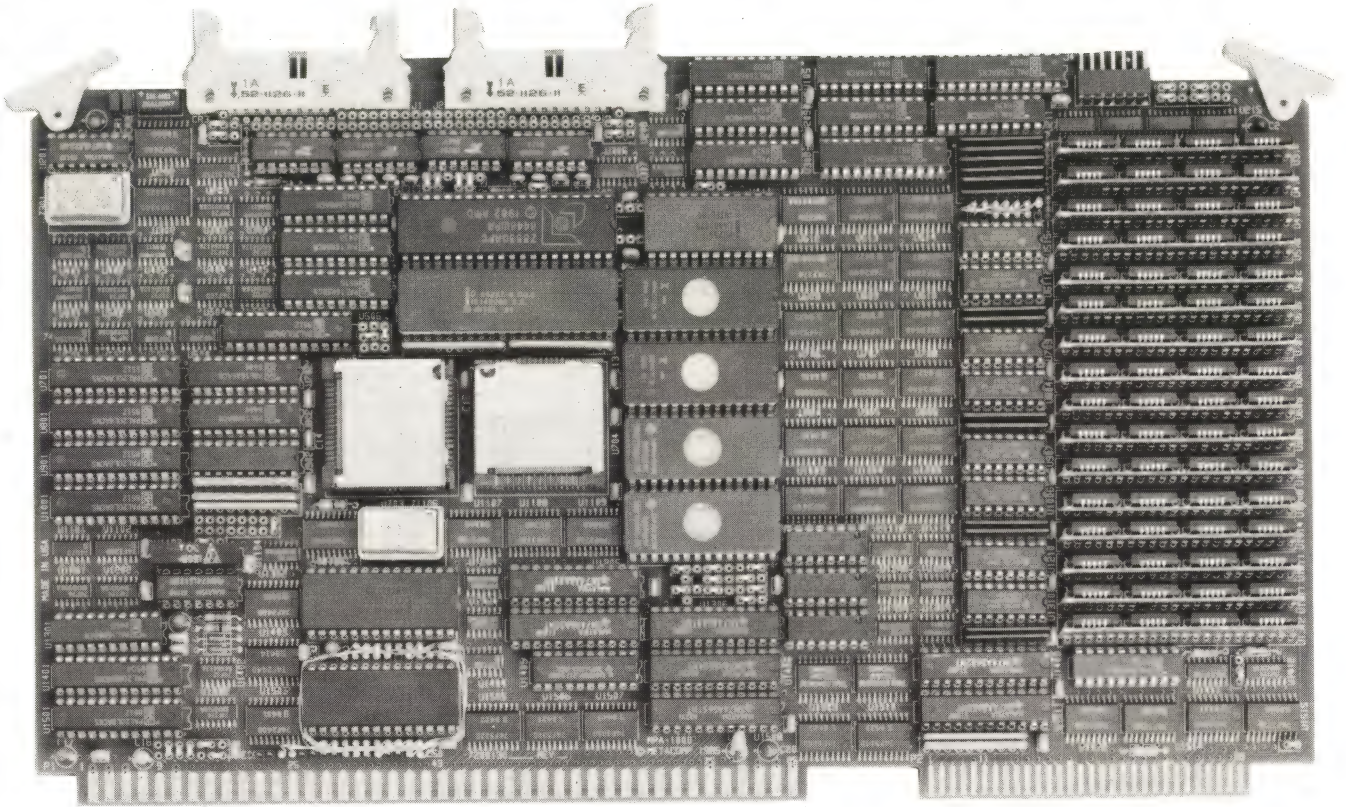
Circle No 365



DISK-STORAGE SYSTEM

The Turbograph DDS-11 disk-storage system performs a number of graphics processing tasks, allowing your host computer to perform other work, and thus improving the efficiency of your graphics system. Based on the manufacturer's HSR-11B graphics processor, the DDS-11 performs vector-to-raster processing. By offloading large graphics data sets onto its dedicated disk system, the system relieves the host CPU of I/O transfer; it then converts the vector data into a raster format to drive an output plotter without further host-CPU interven-

HONEST ENGINE



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The MPA-1000 is the only Multibus-compatible CPU that taps the full capabilities of the 80286 microprocessor. An honest engine, built to unleash the full potential of the 80286 in multi-user, multi-tasking or real-time applications. And it delivers the power and memory for these demanding applications all in a single card slot.

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And for even greater performance, simply plug in the optional 80287 numeric coprocessor and the 82258 Advanced DMA Controller.

Don't compromise. Call or write METACOMP today. Discover what makes the MPA-1000 the honest 80286 engine.

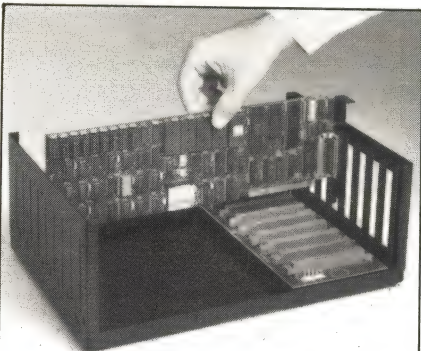
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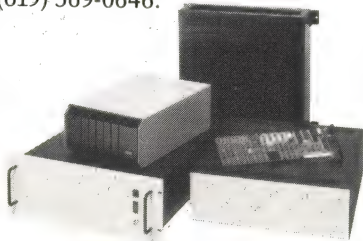
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CIRCLE NO 150

COMPUTERS & PERIPHERALS

tion. You can configure the system with as much as 1G byte of RAM. Built-in plotter interfaces support multipass and specific control requirements to drive your plotter at maximum speed. The DDS-11 supports simultaneous 4-color raster generation, and it provides raster data for multiple copies without regeneration by the host CPU. \$33,000. Delivery, 60 days ARO.

AMF Logic Sciences Inc, 10808 Fallstone Rd, Houston, TX 77099. Phone (713) 879-0536.

Circle No 366



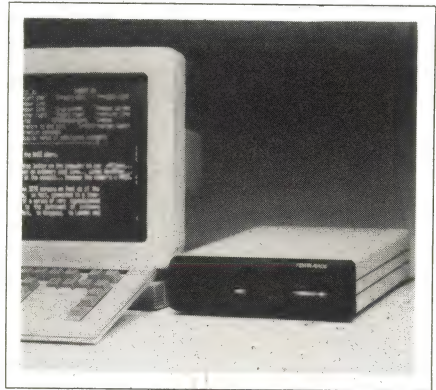
PBX LAN

Providing voice and data communications over twisted-pair wires, the 20-20 PBX offers port-to-port digital transmission at speeds reaching 64k bps. The PBX supports SNA/SDLC, IBM 3270 Bisync, and X.25 protocols. A software editor, accessible from any asynchronous ASCII terminal, lets you alter the networking scheme or make changes in databases locally or remotely. A tandem networking architecture lets you switch voice and data on your internal network, while offering external network options such as on-line satellite communication and WATS. Voice features include an on-line workstation directory, direct inward dialing, off-hook and on-hook call queuing, and music-on-hold. Data transmission features include RS-232C, RS-449/422, and

V.35 interface communication, modem pooling, and support for 960 simultaneous connections. \$400 to \$800 per line.

Harris Corp, Digital Telephone Systems Div, 1 Digital Dr, Novato, CA 94948. Phone (415) 472-2500.

Circle No 367



10k-BPS MODEM

Using data-compression and character-compacting techniques, the Race modem can operate at transmission speeds to 10k bps. When used in conjunction with other kinds of modems, the device offers full-duplex, automatic 300-bps Bell 103 compatibility. A Z80 μ P controls the unit, sensing the degree of data compression that the unit can obtain. By sending variable-length blocks of data at high speeds, terminals and personal computers equipped with Race modems can transmit from 650 to more than 1000 cps. The modem is menu-driven when off line, and provides such features as automatic error correction, autodialing, redialing, and speed modulation. Another version, the Race 2, has an independent printer channel that's statistically multiplexed with the primary output channel so that you can simultaneously receive data on a terminal and output hard copy. Race, \$1995; Race 2, \$2495.

Data Race Inc, 5839 Sebastian Pl, San Antonio, TX 78249. Phone (512) 692-3909.

Circle No 368



Even the smallest bug is big game.

There are no insignificant bugs. They're often ferocious... and elusive!

That's why we built the better "bug hunter." The UDL (Universal Development Laboratory). It's actually an:

- **Advanced 48-channel bus state analyzer**
- **8/16 bit in-circuit emulator**
- **EPROM programmer**
- **Input stimulus generator**

All packed into one, compact box for only **\$2995**.

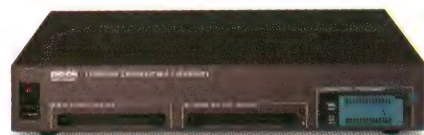
UDL turns almost any PC/MS-DOS and CP/M™ computer into a powerful, integrated workstation for hardware/software debugging. UDL's unique,

real-time emulation lets you track bugs of 46 different target microprocessor "species," without buying expensive hardware adapters.

Access all four instruments through the same control program. Handle single-step debugging with the emulator. And quickly define a complex trigger spec, so the built-in logic analyzer can find those nasty, subtle bugs.

When your tested program is bug-free, plug a PROM into the socket. And with one command, simply write your program from emulation memory directly into the PROM.

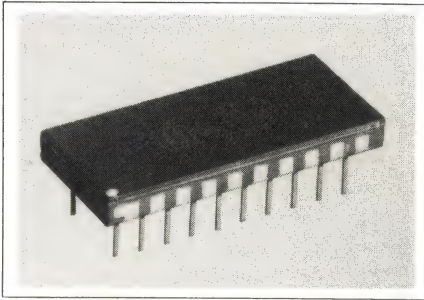
Let our UDL simplify the hunt, and keep you quick on the trigger. If you're serious about bug hunting, find out how to qualify for a no-obligation, 10-day "safari" with UDL. Call: **800/245-8500** (or 415/361-8883 in California). Or write: 702 Marshall Street, 6th Floor, Redwood City, CA 94063.



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CALIBRATOR

The HCAL24010 features 12-bit accuracy over the full range of scaled outputs. Reference input scaling ranges from 1.0 to 0.001. You can use a vernier multiplying scale factor of 1.0, 0.5, and 0.2 within each decade; positive or negative range can be selected digitally. Precision buffers isolate the unit's voltage scaling stages to prevent interaction with polarity, decade, and vernier scaling circuits. The calibrator consists of a unity-gain buffer amplifier and a 2-stage attenuator. The output-voltage-attenuator section is equal to the input voltage at calibrator input times the gain. You can select the value of the gain multiplier with three sets of control lines to determine decade value, vernier value, and sign of the output. \$38 (1000).

Honeywell Inc., Signal Processing Technologies, 1150 E Cheyenne Mountain Blvd, Colorado Springs, CO 80906. Phone (303) 577-1000.

Circle No 369

DELAY LINES

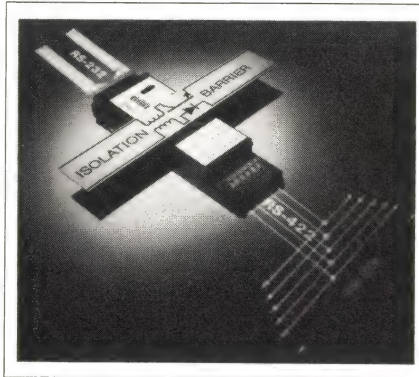
The DS1000 silicon delay lines have five equally spaced taps, providing delays of 20 to 500 nsec, with a tolerance of ± 1 nsec. According to the manufacturer, the devices use less than half the power of conventional hybrid delay lines (35 vs 75 mA). They are available in low-profile, 14-pin DIPs that permit automatic insertion or in 8-pin surface-mount packages. The 100-nsec delay line has a temperature coefficient of less than 300 ppm/ $^{\circ}$ C for both the rising and the falling edges; it oper-



ates over 0 to 70 $^{\circ}$ C. \$3.70 (1000).

Dallas Semiconductor, 4350 Beltwood Parkway, Dallas, TX 75234. Phone (214) 450-0431.

Circle No 370



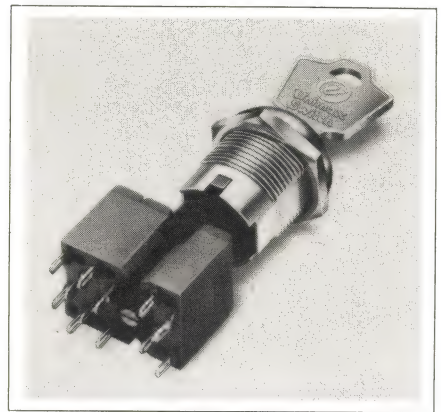
CONVERTER MODEMS

Modems in the LDM422 Series are compact RS-232C-to-RS-422 converters that feature an electrical isolation barrier and heavy-duty electrical-surge protectors. Housed in rugged aluminum enclosures, the modems are small enough to mount on the back panel of most computer equipment. Optical couplers and a dc/dc converter provide isolation. The family is designed for full-duplex operation over two wire pairs plus a ground return. The 3-state outputs permit multidropping of as many as 32 units. Hardware handshaking is available over two additional wire pairs. You can use the second pair as a second full-duplex data channel. One unit may serve as a 2-channel RS-232C/RS-422 converter. Data rates are 75 to 19,200 baud. Six diagnostic LED indicators are provided for installation

guidance and system troubleshooting. The RS-232C interface supports Request to Send, Clear To Send, Data Set Ready, Received Line Signal Detect, and Data Terminal Ready. The RS-422 interface supports Request To Send and Clear to Send on separate wire pairs. From \$111.

Burr-Brown Corp., Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TWX 910-952-1111.

Circle No 371

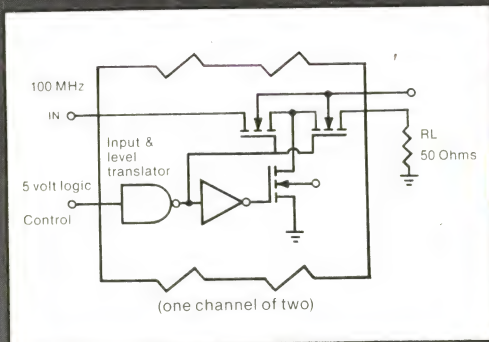


KEYLOCK SWITCHES

The CT Series' separate switch elements and keylocks allow you to preassemble the switch element to its wire leads and the keylock to the panel. At final assembly, the prewired switches slide onto the pre-mounted keylock. The switch elements provide gold-plated, double-break, double-throw contacts rated at 5A/250V ac. Available in single- and double-pole configurations, the UL- and CSA-recognized switch elements allow you to assemble a keylock switch with as many as four poles. Discrete contacts facilitate the switching of different voltages for different circuits. Switches are available in solder, quick-connect, and wire-wrap styles. Mating keylocks are available in 2- and 3-position models with a variety of maintained and momentary key-position arrangements. Each keylock features a 5-disk tumbler-lock mechanism, which offers as many as 100 different keycodes. Key pulls in all maintained key positions are

TOPAZ is DMOS

And DMOS is...



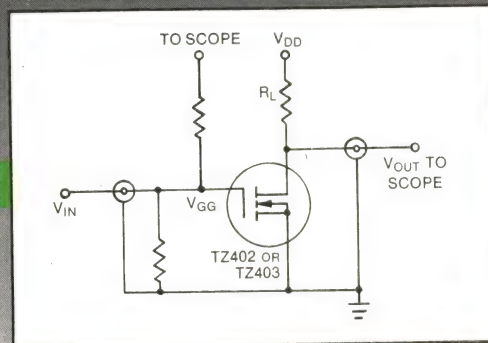
CDG5341-Monolithic CMOS/DMOS "T" switch

... Video Switching

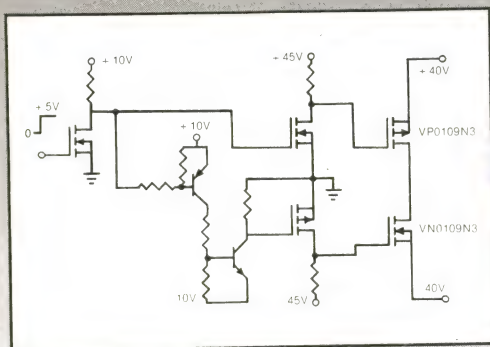
With the lowest capacitance- R_{on} figure of merit, DMOS FETs give you more than 70 db of 'OFF' isolation at 20 MHz (CDG5341). And it's still 55 db at 100 MHz. Combine them with CMOS on the same chip and get an IC that can control ± 10 volts with 5 volt logic. They come as multiplexers... or DPDT switches... or SPDT... or...

... Sub Nanosecond Analog Switching

If fast switching is your thing, then reach for a DMOS. Its input capacitance is so low that driven from a low impedance source, sub nanosecond turn ons... and offs... are easy. Choices of low 'ON' resistances and voltage ranges handle almost every application. And our choice of packages ranges from plastic TO-92's and DIPs through military and custom arrays.



Sub Nanosecond Buffer



Complementary DMOS: Control 80V with 5V Logic

... High Voltage Analog Switching

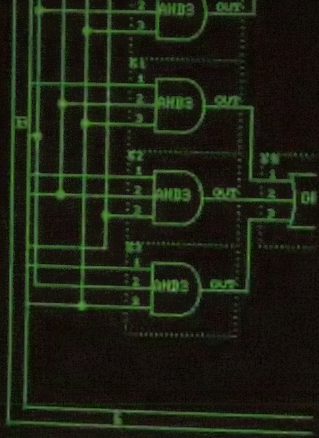
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(617) 964-6205 and ask for Arletta



ABEL(tm) Version 1.13 - Doc
12 to 4 multiplexer
Equations for Module PLD81

Device IC1

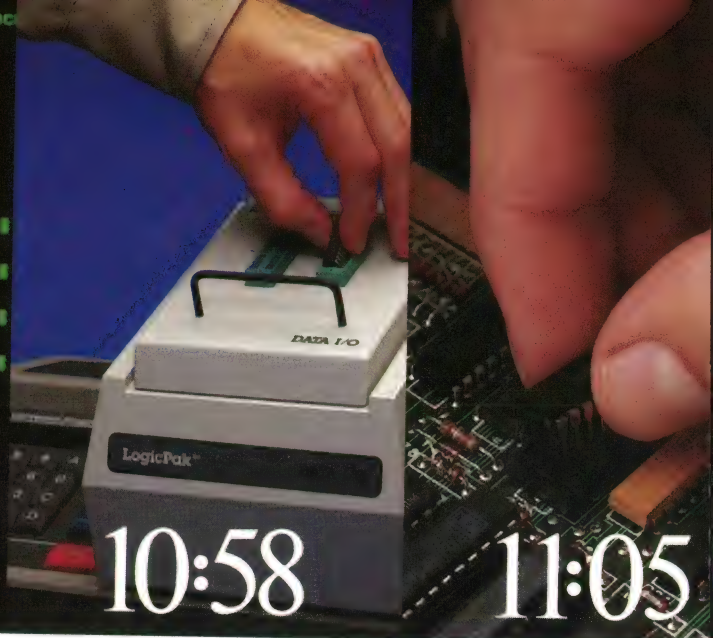
Reduced Equations:

$$Y3 = (A3 \& \text{!}S1 \& \text{!}S2 \&$$

$$Y2 = (A2 \& \text{!}S1 \& \text{!}S2 \&$$

$$Y1 = (A1 \& \text{!}S1 \& \text{!}S2 \&$$

$$Y0 = (\text{!}A0 \& \text{!}S1 \& \text{!}S2 \&$$



8:05

9:37

10:58

11:05

CONCEPT TO SILICON IN 3 HOURS FLAT.

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DATA I/O Japan Ginza Orient Building, 6F, 8-19-13, Ginza Chuo-ku, Tokyo 104, Japan (03) 574-0211/Telex 2522685 DATAIO J

CIRCLE NO 153

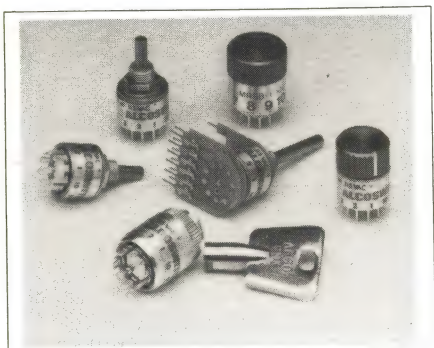
DATA I/O

COMPONENTS & PACKAGING

standard; other key-pull options are available. \$7.30 to \$12 (1000).

Unimax Switch Corp., Ives Rd., Wallingford, CT 06492. Phone (203) 269-8701.

Circle No 372

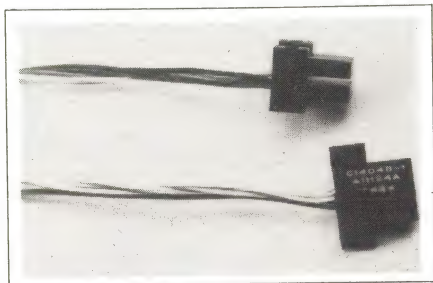


ROTARY SWITCHES

MRS Series miniature rotary switches are available with shaft knob or key actuation and feature as many as three poles and 12 positions. All models have either fixed or adjustable stops. You can order straight or right-angle versions with either lug-type or printed-circuit terminals and gold or silver contacts. The switches have splash-proof, environmentally sealed bodies. The life expectancy of each switch exceeds 10,000 cycles; contacts are rated for 150 mA at 115V ac. PC-mount, 1-pole, 10-position version, \$5.47 (100).

Alco Electronic Products Inc., 1551 Osgood St., North Andover, MA 01845. Phone (617) 685-4371. TWX 710-342-0552.

Circle No 373



OPTICAL SWITCHES

The 112 Series universal optical switches have integral mounting brackets and wire leads for side

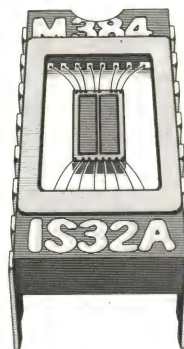
mounting as far as 24 in. from associated circuit boards. Internal hybrid thick-film circuitry provides amplification and wave shaping. An internal LED current-limiting resistor protects the light source. The devices require a 5V dc power input and provide Schmitt trigger outputs capable of driving 10 TTL gates. Single- and dual-channel versions

are available in 0.062-, 0.125-, and 0.188-in. gap sizes. Standard sensor aperture width is 0.015 in. Single-channel version, \$5.21; dual-channel version, \$7.40 (1000). Delivery, 60 days ARO.

HEI Inc., Light Sensing Products Div., Box 5000, Victoria, MN 55386. Phone (612) 443-2500.

Circle No 374

IS32 OpticRAM™



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IS32 OpticRAM™ Quantity Discounts

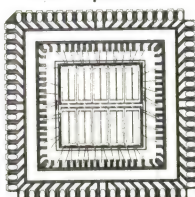
1-24 _____ \$42	100-499 _____ \$30	1000-9999 _____ \$20
25-99 _____ \$34	500-999 _____ \$25	10,000-25,000 _____ \$18

The IS32 OpticRAM™ image sensor is a solid state device capable of sensing an image and translating it to digital computer-compatible signals. Two arrays on the chip each contain 32,768 sensors, arranged as 128 rows by 256 columns. It is a random access device and each sensing element may be uniquely accessed.

Avoid inflated engineering budgets and design with the Micron IS32 OpticRAM™, the affordable design alternative!

Also available is the IS6410 OpticRAM™ cluster chip and the IS256 OpticRAM™. Information and pricing available upon request.

IS6410 OpticRAM™

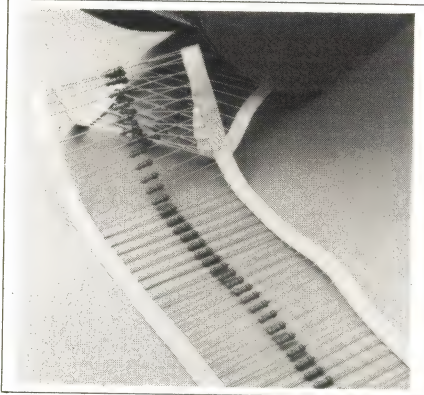


For More Information Contact:

MICRON
TECHNOLOGY, INC.

SYSTEMS GROUP
2805 E. Columbia Rd.
Boise, Idaho 83706
(208) 386-3800
TWX 910-970-5973

"We're building our reputation on innovation."



FILM RESISTORS

The 5053E Series metal film resistors use 50% less pc-board real estate than conventional half-watt resistors, according to the manufacturer. This line can replace the RC20, RN60, and RL20 MIL styles in applications not requiring qualification. The resistor bodies have a maximum length of 0.260 in. and a maximum diameter of 0.098 in. You can place the resistors on 0.350-in. centers. These devices operate over

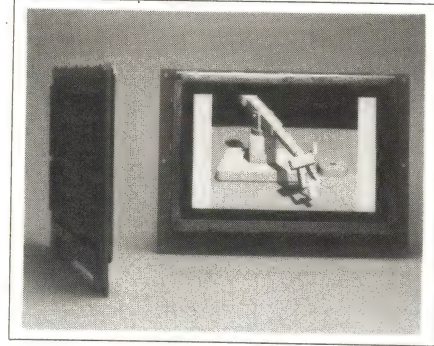
-55 to +155°C and have a maximum operating voltage of 350V rms. With a resistance range of 10Ω to 1 MΩ, resistance tolerance is ±1%, and the temperature coefficient is 100 ppm/°C. With a resistance range of 1Ω to 10 MΩ, resistance tolerance is ±5% at 200 ppm/°C. Power rating at 70°C is ½W. Tape-and-reel packaging is provided for automatic insertion. The 1% resistor, \$16 per 1000 (100,000). Delivery, stock to eight weeks ARO.

Mepco/Electra Inc., Box 760, Mineral Wells, TX 76067. Phone (817) 325-7871.

Circle No 375

DISPLAY

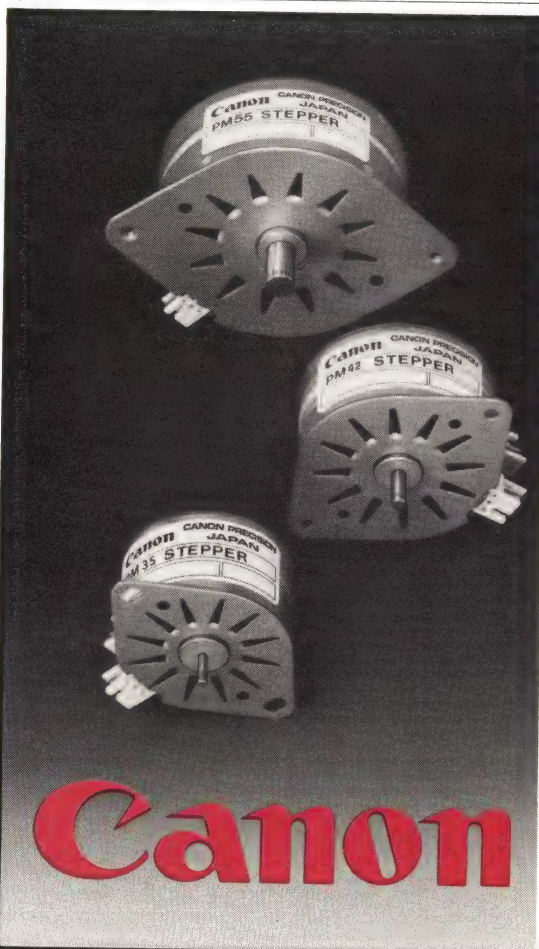
The EL8358 M electroluminescent flat-panel display accommodates graphics, text, and utility software packages created for MS-DOS-compatible computers. According to the company, this is one of the first



flat-panel displays to provide such functions. The device's 640×200-pixel display provides a resolution of 83 lpi with a 5×8-in. active matrix area. A crisp display image individually addresses each pixel, and a 2:1 pixel aspect ratio enhances graphics functions. The display operates over 0 to 55°C. \$775.

Planar Systems, 1400 NW Compton Dr, Beaverton, OR 97005. Phone (503) 690-1100.

Circle No 376



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- Maximum pull-out pulse rates 260 to 720 pps
- Holding torques 110 to 1500 g-cm
- Detent torques 30 to 150 g-cm
- Rotor Inertia 4 to 40 g-cm²
- Weights 100 to 280 grams

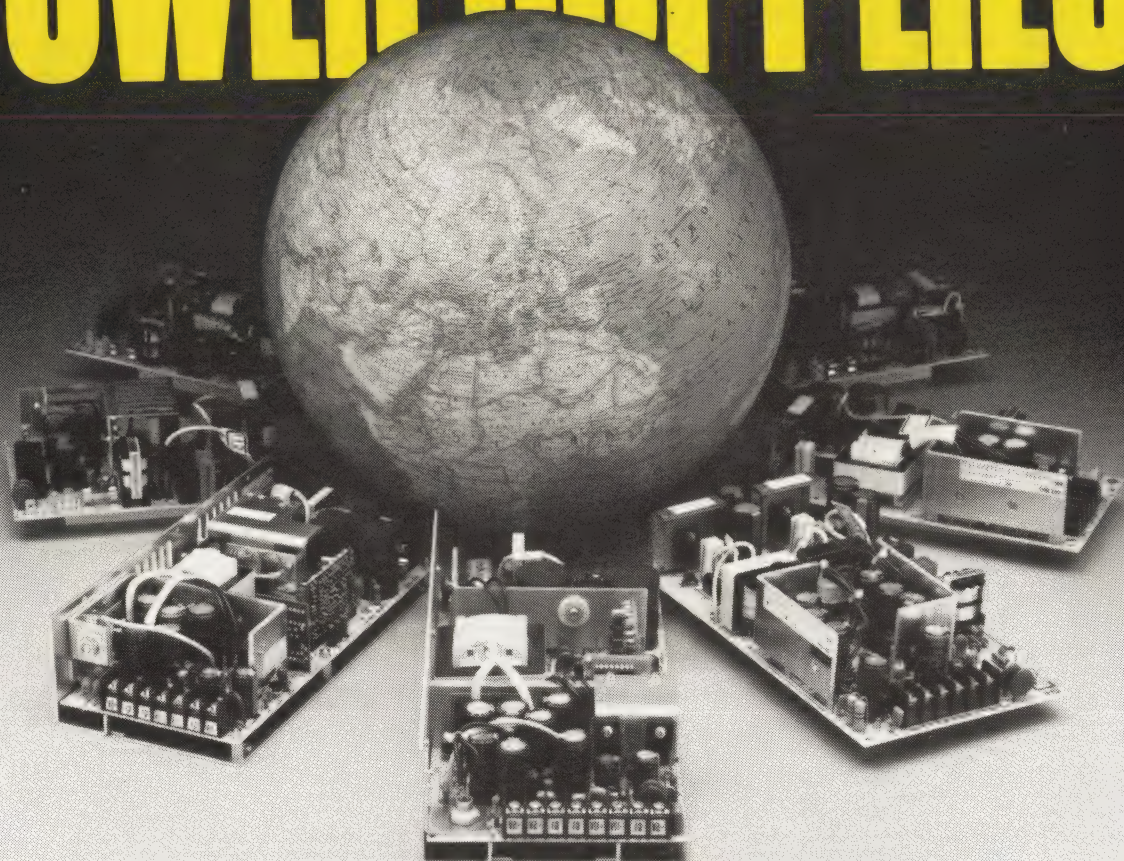
For complete technical information, call or write

CANON U.S.A. INC. Components Division

New York Office/Headquarters
One Canon Plaza
Lake Success, NY 11042
(516) 488-6700 • Telex 96-1333

Santa Clara Office
4000 Burton Drive
Santa Clara, CA 95054
(408) 986-8780 • Telex 17-1961

POWER SUPPLIES



FOR THE WORLD MARKET

KEC now introduces a full-line of multi-output switching power supplies designed expressly for use in OEM equipment that is targeted for sale in the world marketplace.

This new KFD World-Class Series of power supplies includes 23 standard models in 7 different wattages—25W, 40W, 60W, 80W, 100W, 130W and 200W—plus customer specials. All are designed to meet VDE, IEC, UL, and CSA safety requirements; and EMI emissions are in compliance with VDE/FCC specifications. All models are engineered for full-time duty at their maximum rated outputs. (We build in the safety margins you need, so you don't

have to overspecify a unit to get one you can trust.)

The small size and low-profile PC board style of these new units allow them to be fitted into very compact spaces, making them ideal for use with microperipheral equipment. Despite their superior design, their construction of the finest materials, and their full two-year warranty—these new world-class KFD switching power supplies are available at low-cost highly competitive prices.

For full specifications, send for the KEC KFD Series product brochure. **KEC Electronics, Inc.**, 20817 Western Avenue, Torrance, California 90501, (213) 320-3902.



KEC ELECTRONICS, INC.

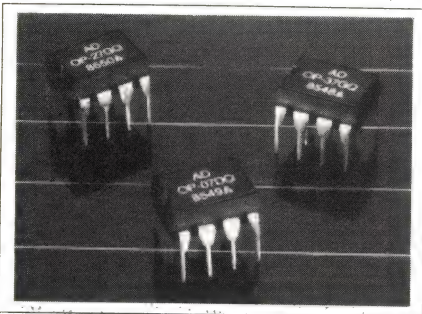
NEW PRODUCTS: ICs & SEMICONDUCTORS

CODEC ICs

These TTL-compatible, monolithic PCM codec ICs, the HC-5510 and -5511, use a proprietary, double-poly CMOS process that provides low-noise operation over 0 to 75°C. Each device contains separate A/D and D/A circuitry and sample/hold capacitors. A serial control port allows an external controller to individually assign the PCM input and output ports to one of 32 time slots, to place the codecs in a power-down mode, or to operate them in a fixed time-slot mode. The HC-5510 uses μ -Law coding for Bell-compatible signaling; the -5511 uses A-Law coding for European or CCITT applications. The HC-5510 comes in a 24-pin ceramic DIP; the HC-5511 comes in a 22-pin package. \$10.45 (100).

Harris Corp., Semiconductor Sector, Box 883, Melbourne, FL 32901. Phone (305) 724-7800.

Circle No 377



PRECISION OP AMPS

This manufacturer's OP-07, -27, and -37 precision op amps come in hermetically sealed 8-pin DIPs; earlier versions are available in plastic DIPs and TO-99 metal cans. Identified by a Q suffix, the units suit military as well as industrial environments; you can order them screened to MIL-STD-883B. Each amp offers grades characterized for different performance levels over temperature. For each type's highest grade, maximum specifications for offset voltage, offset-voltage drift, and long-term stability are guaranteed at 25 μ V, 0.6 μ V/°C, and 1.0 μ V/month, respectively.

The OP-07Q specs a closed-loop bandwidth of 0.6 MHz typ and a maximum input noise of 0.6 μ V p-p (0.1 to 10 Hz). The -27Q's maximum input noise is 0.18 μ V p-p (best grade); its minimum gain-bandwidth product is 5 MHz (all grades). The -37Q also guarantees input noise of 0.18 μ V p-p; however, its minimum gain-bandwidth product is 45 MHz (all grades). -07Q, \$1.80 to \$18.35; -27Q and -37Q, \$3.80 to \$20.70 (100).

Analog Devices Inc., 70 Shawmut Rd, Canton, MA 02021. Phone (617) 935-5565.

Circle No 378

RAM CONTROLLER

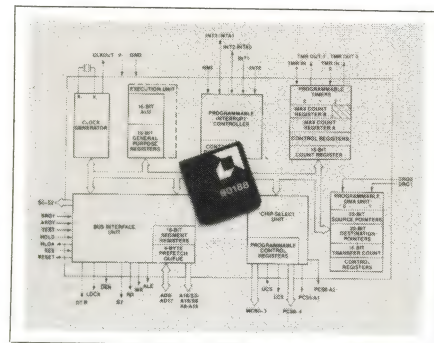
Using low-power-Schottky TTL technology, the MB1422 operates with clock periods as short as 80 nsec and dissipates 440 mW from a 5V supply. The dynamic-RAM controller provides an interface to both memory chips and μ Ps. On the memory side, it doesn't require extra drives to provide addressing and refresh for as many as 44 RAMs; on the μ P side, it supports both 5- to 8-MHz 8086s and 8- to 12.5-MHz 68000s. You can choose either internal or external dynamic-RAM refresh. The internal mode handles refresh timing and addressing automatically. In the external mode, the controller still generates addresses, but an external signal triggers each refresh cycle. In a 42-pin plastic DIP, \$9.75 (1000).

Fujitsu Microelectronics Inc., 3320 Scott Blvd, Santa Clara, CA 95054. Phone (408) 727-1700. TWX 910-338-0190.

Circle No 379

PLCC μ P

The manufacturer claims that it has reduced design-in costs by 25% by packaging its 80188 8-bit μ P in a plastic leaded chip carrier. The μ P combines five iAPX86 system components on one chip. According to the company, the device offers



twice the performance of the standard 8088 μ P. The 80188 is upward compatible with 8086 and 8088 software and has 10 more instructions than are in the 8088 instruction set. Six- and 8-MHz versions are available. The μ P also comes in an LCC package and a pin-grid-array package. 8-MHz version, \$19.95 (100).

Advanced Micro Devices Inc., Box 3453, Sunnyvale, CA 94088. Phone (408) 982-7445.

Circle No 380

A/D CONVERTERS

The 6-bit Model HA19216 and the 8-bit Models HA19210/209 provide conversions of 3M samples/sec and operate from single 5V supplies. The HA19216 incorporates latched 3-state data outputs and clock-input terminals that are TTL and CMOS compatible. Housed in an 18-pin DIP, the device dissipates 270 mW typ. Linearity error is ± 0.25 LSB typ. The HA19210/209 converters are enclosed in 28-pin packages, spec a typical linearity of ± 0.5 LSB, and dissipate 250 mW typ. Input-clock levels and digital-output signal levels are TTL and CMOS compatible. The difference between the two units is the output state in an overflow condition: During an overflow, all outputs are logic zero for the HA19210 and logic one for the HA19209. 6-bit model, \$14.40; 8-bit models, \$26.40 (plastic) and \$36 (ceramic) (1000).

Hitachi America Ltd., Semiconductor & IC Div, 2210 O'Toole Ave, San Jose, CA 95131. Phone (408) 942-1500. TLX 171581.

Circle No 381

Curvette™. Now VDE certified.

Curvette—Ready for Export. Our new curved rocker offers several dramatic improvements over standard switches. Some you can see, some you can't . . .

A European Shape. Outside, the Curvette has a compound curve bezel that blends into the panel. No hard edges. Rounded corners. A soft, glare-free matte finish. Choice of color. The look is clean and contemporary.

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We'll send you a sample Curvette FREE. You'll see for yourself what an improvement Curvette is — with more performance and protection for the lowest cost you'll find anywhere.

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CARLINGSWITCH
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CIRCLE NO 157

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And the dryfit® name means you'll never again have a good design blamed when a questionable battery was at fault. dryfit delivers the longest, most reliable service life of any sealed lead-acid battery in the world. From four to eight, or even more absolutely maintenance-free years, depending on the model needed for your cycling or float application. For example, Sola Electric recently chose our 12 volt 28Ah battery for their SPS and UPS equipment.

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If that's still not enough to convince you,

consider these advantages. Leakproof construction, resealable safety vents, low space requirement, operation over a wide temperature range, simple "no fill or charge needed" installation. And the shock and vibration characteristics to survive the abuse of an armored tank.

Why trust us?

Just check our credentials! dryfit batteries are made by Sonnenschein, inventor of the original gelled electrolyte battery system. With more different battery types, dryfit outnumbers all the competition. No wonder it has been Europe's most popular battery for decades!

And now, adding value to your good name is as easy as calling ours:

1-800-4dryfit

Exclusive Canadian Agent:
Duracell, Inc., Mississauga



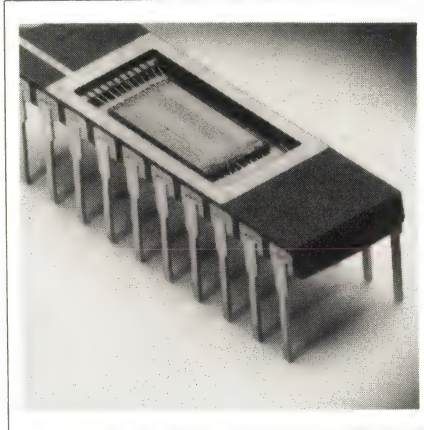
P.O. Box 339
300 East Johnson Avenue
Cheshire, CT 06410
(203) 271-0091

FET BUFFER

The MP2004 is a 350-MHz FET buffer that's suitable for unity-gain applications requiring currents as high as 100 mA. When used inside op-amp feedback loops, its 2500V/ μ sec slew rate and wide bandwidth ensure circuit stability. The buffer replaces National Semiconductor's LH0033 and functions as an inverting amplifier for the manufacturer's 6- and 8-bit flash converters (MP7682, 7683, and 7684). It specs ± 5 to ± 15 V operation, a 1-nsec rise time, 2.5-nA input current (warm), and 250-mA peak output current. From \$20.85 (100).

Micro Power Systems Inc., 3100 Alfred St, Santa Clara, CA 95054. Phone (408) 727-5350. TWX 910-338-0154.

Circle No 382

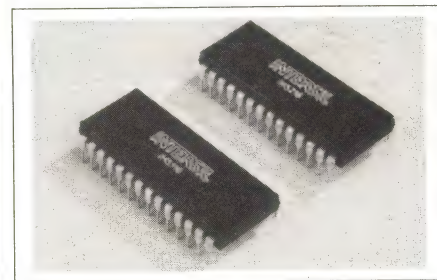


64k-BIT STATIC RAM

The SR64K4 CMOS static RAM has an access time of 45 nsec max over the military temperature range. (The part is already available in a 35-nsec access-time version for operation over the commercial temperature range.) The RAM uses temperature-compensated substrate-bias techniques, depletion devices (not usually found in CMOS ICs), and special decoupling circuits, all of which contribute to speed derating of less than 1 nsec per 10°C . It's organized as $16\text{k} \times 4$ bits and costs \$330 (1000). A 55-nsec version is available for \$285 (1000).

Lattice Semiconductor Corp., 15400 NW Greenbriar Parkway, Beaverton, OR 97006. Phone (503) 629-2131.

Circle No 384



MULTIPLEXER

The IH5116/5216 16-channel CMOS multiplexer offers full fault protection. According to the company, all channels turn off during power failure to protect the transducers and the multiplexer. Moreover, no transducer crosstalk exists. The part limits output signals to levels 1.5V lower than the supplies. During fault or undervoltage conditions, no excessive current drain results. When the power is off, the multiplexer protects against input voltages as high as ± 40 V. The device is TTL compatible (including enable) and comes in a ceramic or plastic DIP. In plastic, \$18.90 (100). Delivery, four to six weeks ARO.

Intersil Inc., 10600 Ridgeview Ct, Cupertino, CA 95014. Phone (408) 996-5582.

Circle No 383

ANALOG SWITCHES

The DG400 family of monolithic analog switches features low on-resistance (20Ω typ and 25Ω max) and fast switching (maximum $t_{\text{ON}}=125$ nsec and $t_{\text{OFF}}=75$ nsec for A grade). The switches consume $35\mu\text{W}$. They are available in spst, spdt, and dpdt versions, as well as in single- and dual-switch packages. Optional housing includes 16-pin plastic and ceramic DIPs. The spdt versions guarantee break-before-make switch action, which ensures that independent sources aren't shorted together during changeover. On-resistance is stable over the full analog-input range of ± 15 V; according

2

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MODEL SELECTION CHART

	MAIN OUTPUT			
	No. 2 OUTPUT			
	No. 3 OUTPUT			
	No. 4 OUTPUT			
RMV220: CONVECTION COOLED 220W				
RMV223B-2330	5V	12V	12V	N/A
RMV224B-2332	5V	12V	12V	5V
RMV224B-2339	5V	12V	12V	24V
RMV224B-2449	5V	15V	15V	24V
RMV224B-2333	5V	12V	12V	12V

RMC 300: AIR COOLED 300W*

RMV 300: CONVECTION COOLED 300W*

RMC 400: AIR COOLED 400W*

*Same selection as chart above.

For immediate assistance
call (619) 439-4200.

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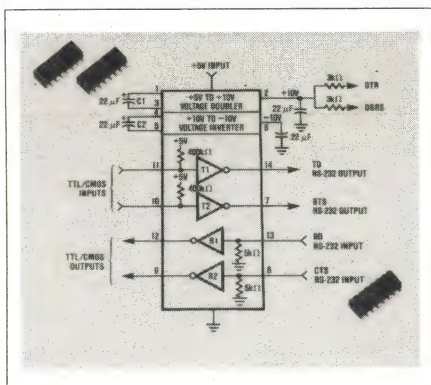
401 Jones Road, Oceanside, CA 92054.
Tel: 619/757-1880. TLX: 350227

ICs & SEMI- CONDUCTORS

to the supplier, this flatness rivals the performance of JFET designs. \$4.06 to \$20.70 (100). Delivery, six weeks ARO.

Siliconix Inc., 2201 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 988-8000.

Circle No 385



TRANSCEIVER

The MAX232 meets EIA RS-232C specifications. It operates from one 5V supply and replaces the $\pm 12V$ supplies and two interface ICs commonly used in RS-232C communication links. The transceiver comprises a voltage-converter block that transforms 5V to 10V and +10V to -10V, dual RS-232C transmitters, and dual RS-232C receivers. The $\pm 10V$ charge-pump voltage converters use four external electrolytic capacitors; the converters' chopping frequency is internally set to 16 kHz. The transmitter inputs are TTL and CMOS compatible, and the logic threshold is set at 1.3V when $V_{CC}=5V$. The outputs' slew rate is limited to a value less than $30V/\mu\text{sec}$. Powered-down output impedance is 300Ω min when V_{CC} equals 0V and $\pm 2V$ is applied to the outputs. Input impedance is between 3 and 7 k Ω . \$3.60 to \$7.20 (100).

Maxim Integrated Products, 510 N Pastoria Ave, Sunnyvale, CA 94086. Phone (408) 737-7600.

Circle No 386

NEW!

A LOW PROFILE PCB SWITCH...



that's also watertight

The new Series 98 from EAO has the great styling of a low profile control with an important difference: it's the only low profile PCB switch that's completely sealed. Built to IP-67 standards (similar to NEMA 4 and 13), this newest EAO switch remains watertight in up to 3 feet of water at temperatures from -25°C to $+85^{\circ}\text{C}$.

Watertight seals aren't all. The Series 98 has gold plated, low bounce contacts with an estimated lifetime of 5 million operations. Rated at 50 VAC/72 VDC @ 100mA; 3W maximum, it's available in three sizes and several configurations including non-illuminated, illuminated with one or two LED's, momentary or maintained action (Form C), four cap colors and a film insert.

Stop fishing around. Now EAO has a great looking, low profile control with the added security of a watertight seal. It's your ideal catch!

EAO Switch. You can feel the difference.

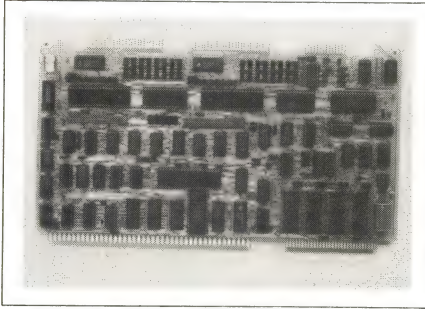
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NEW PRODUCTS: COMPUTER-SYSTEM SUBASSEMBLIES



SINGLE-BOARD μ C

The CBC 85C/24 CMOS Multibus CPU card is compatible with Intel's iSBC 80/24 but requires 5% of the 80/24's operating current, according to the company. The single-board computer features an 80C85 μ P operating at 2.42 or 4.84 MHz, 8k bytes of CMOS static RAM, sockets for as much as 64k bytes of JEDEC-compatible EPROM, 48 parallel I/O lines, two programmable 16-bit counter/timers, a programmable serial interface, and two SBX-compatible connectors. An onboard lithium battery provides five years of continuous RAM data retention. The board is available in two versions for operation over 0 to 70°C or -40 to +85°C. Power consumption is 150 mA at 5V. \$945.

Diversified Technology Inc., Box 748, Ridgeland, MS 39158. Phone (601) 856-4121. TLX 585326.

Circle No 387

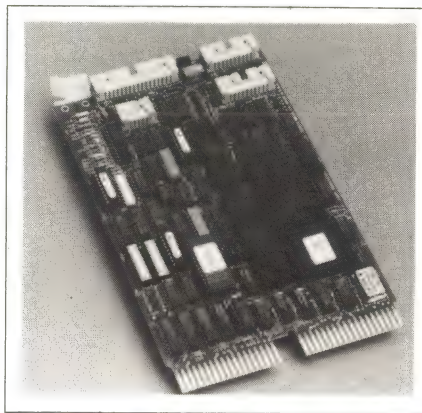
MULTIFUNCTION BOARD

The X2C multifunction board for the IBM PC and PC/XT features a serial port, a parallel port, a game port, and as much as 2M bytes of additional main memory. It also offers programs for self-booting and advanced diagnostics. With the RAM disk feature, which emulates a disk drive, plus an external ac adapter power pack, you can preserve data on RAM disks indefinitely when the computer's power is shut off. Lotus/Intel/Microsoft EMS permits such programs as Lotus 1-2-3, Symphony, and Ashton-Tate Framework to access the 2M bytes of RAM on the card. An EMS memory-manager driver is included. A

pop-up windowing spooler, accessible from within an application program, allows you to pause, resume, or cancel printing, print multiple copies, or send control codes to the printer. A security feature is optional. You don't need to set any switches to install the board. \$395.

ABM Computer Systems, 3 Whatney, Irvine, CA 92718. Phone (800) 372-8400; in CA, (714) 859-6531. TLX 292427.

Circle No 388

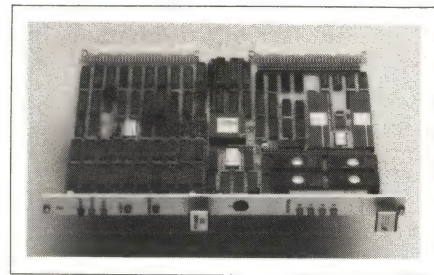


DISK CONTROLLER

This dual-height μ P-based disk controller, the QDO1/D, can interface two ST506 5 1/4-in. Winchester disk drives with the Q Bus. The controller emulates DEC's mass-storage control protocol and is compatible with the MicroVAX I and II, LSI-11, and MicroPDP-11. Data transfers are facilitated by block-mode support and adaptive DMA, which releases the bus to other DMA devices with a lower priority, based on bus requests. Noninterleaved sectors enable large data transfers from contiguous sectors. The nonvolatile static RAM stores drive configurations, and a command buffer prioritizes commands for enhanced throughput. The controller provides 48-bit error-correction code and 16-bit cyclic redundancy check for error detection. \$1122 (100).

Emulex Corp., Box 6725, Costa Mesa, CA 92626. Phone (800) 368-5393; in CA, (714) 662-5600.

Circle No 389

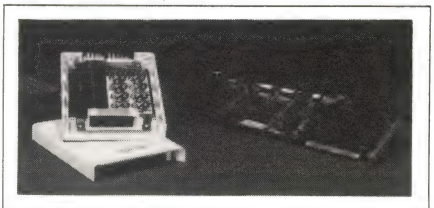


VME BUS COMPUTER

The PT-VME102 single-board VME Bus computer is based on the 68010 μ P running at 10 MHz. It's available with either 512k or 2M bytes of onboard dynamic RAM; you can upgrade the 512k-byte version to 2M bytes. The company's Multiport facility permits concurrent operation of the 68010 MPU, with onboard ROM or module-based I/O, while the VME Bus is accessing the dynamic RAM. In addition to support for as much as 256k bytes of ROM, the board features a 7-level software-configurable interrupter, a 7-level interrupt handler, and two serial asynchronous/synchronous ports. Ten defined I/O Paks permit the addition of a 68881 floating-point processor; a SCSI interface with or without DMA; as many as six serial I/O ports with or without DMA; or a Centronics port. 512k-byte version, from \$2195; I/O Paks, \$200 to \$895.

Performance Technologies Inc., 300 Main St, East Rochester, NY 14445. Phone (716) 586-6727.

Circle No 390



DATA-ACQUISITION CARD

Model ACPC-12, a 12-bit data-acquisition card for the IBM PC and compatibles, features an integrating A/D converter and automatic zero and full-scale calibration. It reads data into memory at speeds to 25 kHz. You can connect any combination of inputs from a variety of

WHERE PERFORMANCE COUNTS

Northrop Electronics Division is a highly focused organization building on strong performance in guidance and navigation. Software and Inertial Systems Engineers apply their expertise to advanced electronic projects that are unequaled in accuracy. These projects include the Advanced Inertial Reference Sphere which has met all performance specifications and the Ring Laser Gyro, another key technology ensuring continued success and growth. Make your performance count through the following opportunities:

TEST SYSTEMS DESIGN AND DEVELOPMENT

ATE Software Development Engineer

Develop software for control of ATE. Analyze requirements and develop design descriptions, functional flowcharts and module subroutine allocations, code and integrate. Requires experience with HP-2000 series computer and working knowledge of Pascal and FORTRAN; experience with HP Data Acquisition Control Unit 3497 desired. BSEE required.

ATE Specifications Engineer

Develop specifications for ATE hardware and software in accordance with MIL-STDs 490 and 483. Requires knowledge of ATLAS and experience with ATE or test program sets. MIL-STDs 490 and 483 background preferred. BSEE required.

ATE Systems Software Engineers

Design, code and integrate software modules relating to ATLAS compiler and test station operation system for automated test systems, working from new ATS requirements or change requests. Requires experience with HP-1000 automated test systems, HP RTE IVB, HPID and HP device subroutines, related software and ATLAS compilers. Fluent knowledge of FORTRAN IV required. BSEE, BSCS, MS/Math or equivalent experience required.

Metrology Engineer

Assume lead role in development and integration of a mobile automatic calibration system for depot ATE. Define calibration requirements, select standards and develop procedures. Assist in the development and implementation of ATE calibration software. BSEE and at least 7 years' experience required.

Please send your resume to: Melanie Graper

DIGITAL IMAGE PROCESSING ENGINEERS

Design hardware/firmware for real-time image processing systems. Position requires extensive knowledge of digital/signal processing hardware and background knowledge of FFT algorithms and other image processing techniques. Requires at least 3 years of digital signal processing experience in both hardware and software/firmware design disciplines. BSEE or BSCS minimum, MSEE/MSCS preferred.

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- Signal Signature Logic
- Diagnostic Flowcharts

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Function as key decision makers and the liaison between precision design and avionics manufacturing units in solving design, MRB, PCB, flex-harness, hybrid and other electrical/material problems that occur during the transition from design to the production of precision electro-mechanical assemblies. Position requires BSEE or MSEE and minimum 5 years' experience related to PCB design technology and manufacturing processes with emphasis on flex-harness and hybrids.

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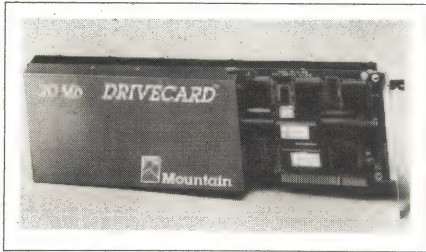
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COMPUTER-SYSTEM SUBASSEMBLIES

sensors. Cold-junction compensation and linearization for thermocouples is provided. Inputs are protected to 150V. Full-function, menu-driven applications software is also included. From \$790.

Strawberry Tree Computers, 1010 W Fremont Ave, Sunnyvale, CA 94087. Phone (408) 736-3083.

Circle No 391



HARD-DISK CARD

DriveCard is an internal 10M- or 20M-byte hard-disk-drive system that requires one-and-a-half card slots. It features a 3½-in. Winchester disk drive and can be used with

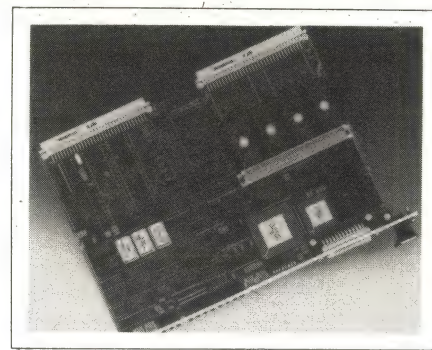
the IBM PC, PC/XT, and compatibles. The half-slot portion of the unit fits the nonconnector half of a full card-cage slot, leaving the connector open to accept another half card. The unit consumes 15W from the computer's power supply. The company's hard-disk utilities software is included, and the system carries a 1-year warranty. 10M-byte version, \$995; 20M-byte version, \$1195.

Mountain Computer Inc, 360 El Pueblo Rd, Scotts Valley, CA 95066. Phone (800) 485-0300; in CA, (800) 821-6066.

Circle No 392

32-BIT CPUs

The CPU-20/21 are 32-bit VME Bus boards that run at 16.7 MHz without wait states and access as much as 1M byte of high-speed local static RAM. The CPU-21 includes a 68881 floating-point coprocessor. Each



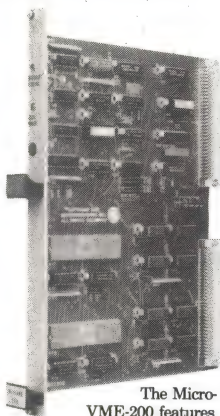
board provides one RS-232C-compatible port for use as a debug port and an RS-232C or RS-422 general-purpose interface. Additional features include 256k to 1M bytes of no-wait-state static RAM, four 32-bit-wide EPROM sockets, four 32-bit-wide EPROM or static-RAM sockets, and sockets for as much as 512k bytes of onboard EPROM. From \$5450.

Force Computers Inc, 727 University Ave, Los Gatos, CA 95030. Phone (408) 354-3410.

Circle No 393

Low-Cost VMEbus I/O Modules

The MicroVME™ family of I/O modules offers you a choice of VMEbus I/O options — at a reasonable price. All are designed to simplify your system design. I/O's are routed through the P2 connector for easy service — with no I/O cables to clutter up your front panel. Software driver source code, peripheral chip manuals and a complete MicroVME manual are included.



The MicroVME-200 features 32 TTL I/O lines, 2 timers and more

MicroVME-200 Features

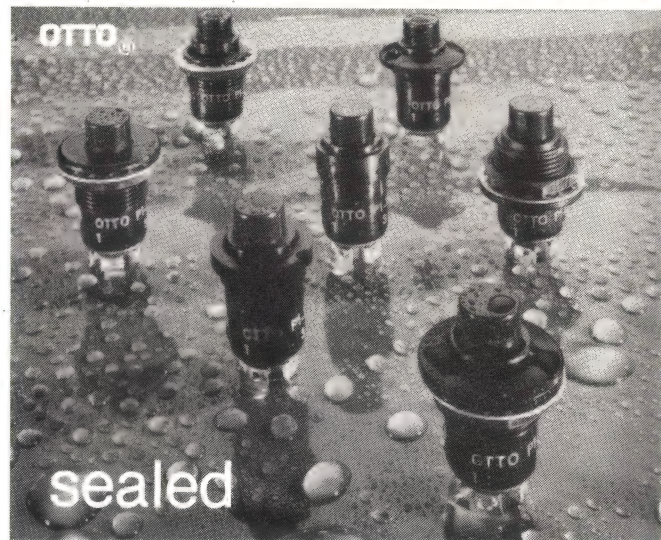
- VMEbus A16:D8 DTB Slave
- 7 Level interrupt capability
- All I/O through P2 connector
- 32 programmable TTL I/O lines, buffered in groups of 4
- 8 handshake/interrupt lines
- Dual Eurocard format
- Flexible addressing
- 2 24-bit timers
- OPTO-22® compatible

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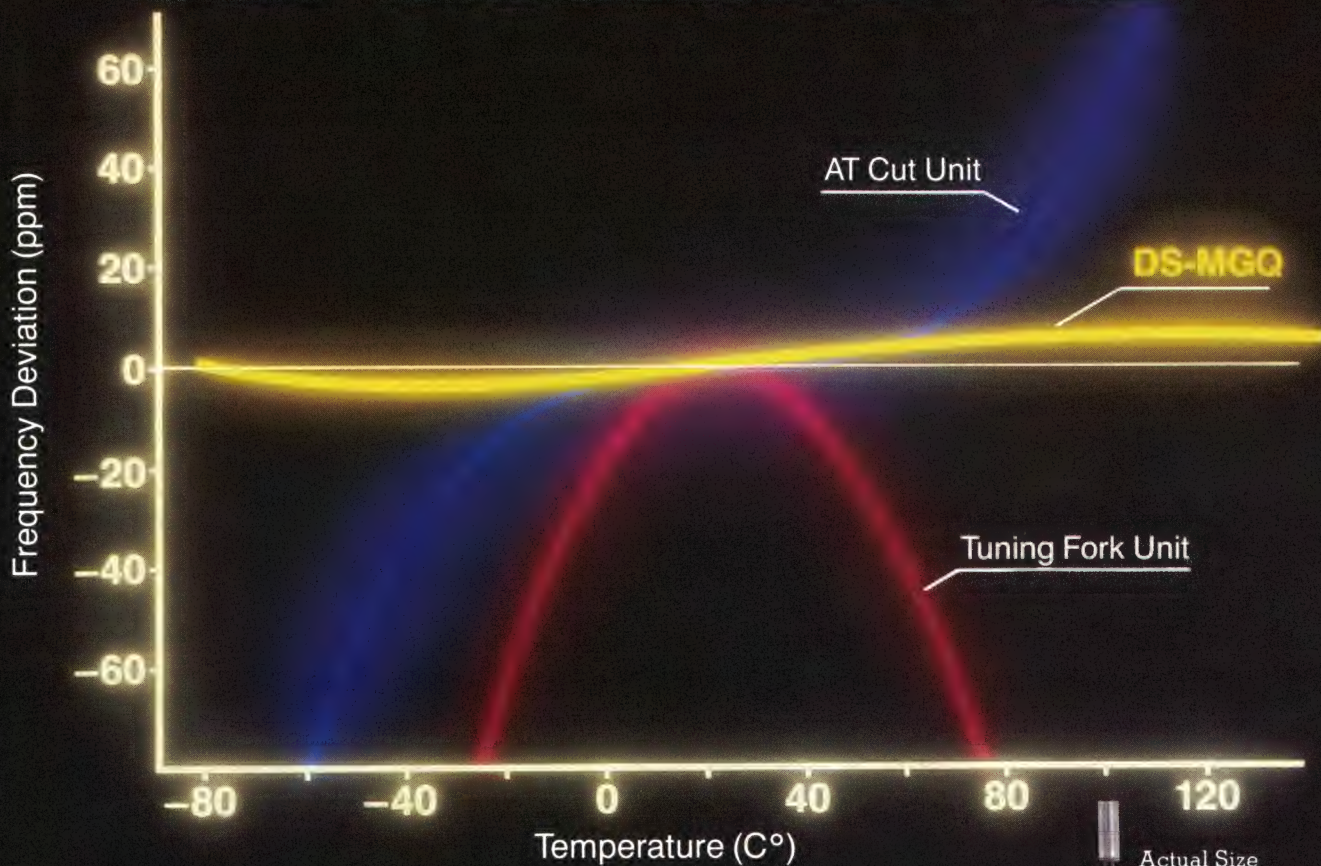
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Moisture and dust are sealed out with OTTO's new internal silicon rubber rolling sleeve at button; epoxy at case and terminals. Positive tactile feed-back actuation. High contact pressure patented design assures < .025 Ω contact resistance for dry circuits while offering a big 10 ampere rating. Available in a variety of bezels and contact arrangements, in MIL-S-8805 and commercial construction. Write for Catalogs P1 and P3. Call for samples.

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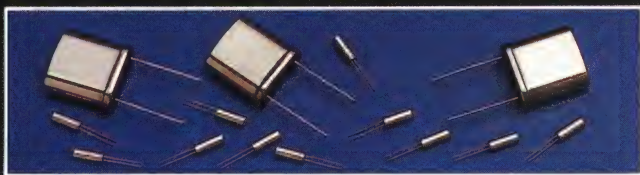
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the exciting possibilities in your present and planned products. Then write or call today for specifics.

KEY SPECIFICATIONS

Frequency Range	1.0 to 3.0 MHz
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Quality Factor	150,000 to 300,000*
Effective Series Resistance	35Ω to 100Ω*
Frequency Temperature Stability (-30°C to +70°C)	± 5ppm to ± 100ppm
Drive Level (Max)	3 to 20μW*
Aging (First Year +25°C)	1.0ppm (typical)

*Depending on Frequency

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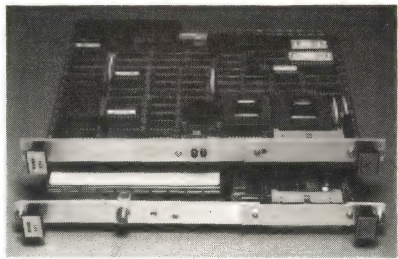
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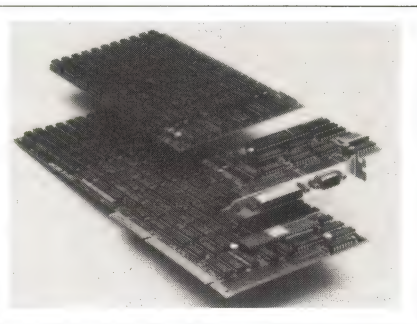


CONTROLLER

The MC68605 X.25 protocol controller (XPC) implements the CCITT Recommendation X.25 data-link-access procedure in switched data-communication networks, high-level data-link control (HDLC) master/slave networks, and high-speed computer-to-computer communications. The controller generates X.25 link-level commands and responses, or you can manually implement X.25 protocols. Shared memory structures allow you to queue an unlimited number of receive and transmit frames, each containing as much as 64k bits of data. The controller handles full-duplex, synchronous serial data at rates to 10M bps max; the system clock rate is 12.5 MHz max. You can choose an 8- or a 16-bit data bus. Samples are available now; production quantities, this quarter. 84-lead pin-grid-array package, \$86.

Motorola Inc., Semiconductor Products Sector, Box 6000, Austin, TX 78762. Phone (512) 440-2839.

Circle No 394



EXPANSION BOARD

The Eccell expansion board for the IBM PC/AT features the Lotus/Intel/Microsoft EMS, an error-correction system that automatically detects and corrects memory er-

rors. The board provides a menu-driven installation program and a disk-caching feature, which, according to the company, speeds disk access by as much as 10 times over normal disk-drive access. Additional features include a warm-boot facility, which allows you to reboot the PC/AT without having to reload the RAM disk, and a print-spooling pro-

gram. The board provides a memory capacity of 1M byte on the main card and 2M bytes on the optional daughter card, for a total of 3M bytes per board. \$595; daughter card, \$145.

Orchid Technology, 47790 Westinghouse Dr, Fremont, CA 94539. Phone (415) 490-8586.

Circle No 395

Simplify your μ P-DAC designs

ALL DAC811 NEEDS TO INTERFACE TO YOUR MICROPROCESSOR... IS YOUR MICROPROCESSOR!

Why add extra size, cost, design time, and parts to your microprocessor systems when you can use DAC811?

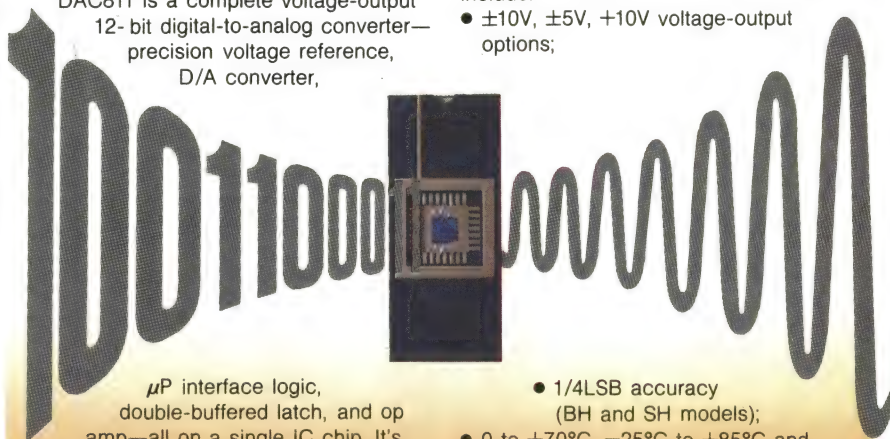
A Complete Solution

DAC811 is a complete voltage-output 12-bit digital-to-analog converter—precision voltage reference, D/A converter,

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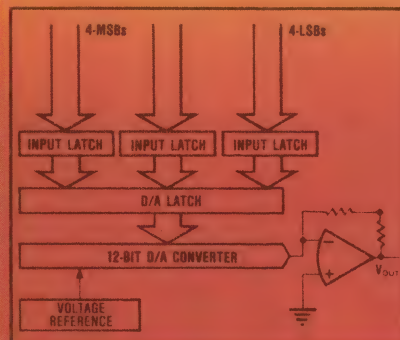


μ P interface logic, double-buffered latch, and op amp—all on a single IC chip. It's designed to make your DAC- μ P interfacing circuits—4-, 8-, 12- and 16-bit buses—simple and trouble-free, with no extra parts needed, very economical pricing, and significant board space savings.

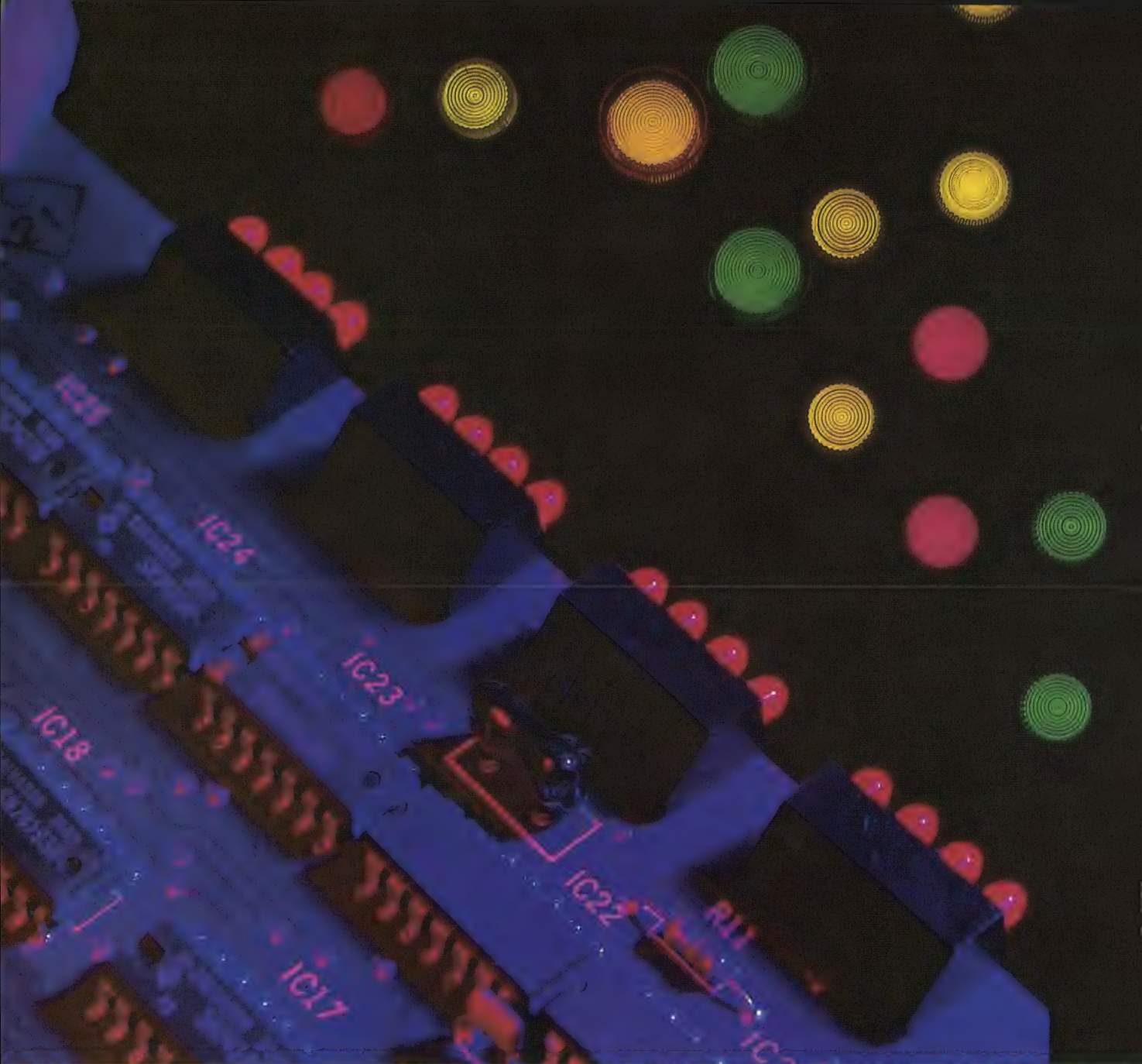
- 1/4LSB accuracy (BH and SH models);
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Burr-Brown Corporation, PO Box 11400, Tucson, AZ 85734. (602) 746-1111.



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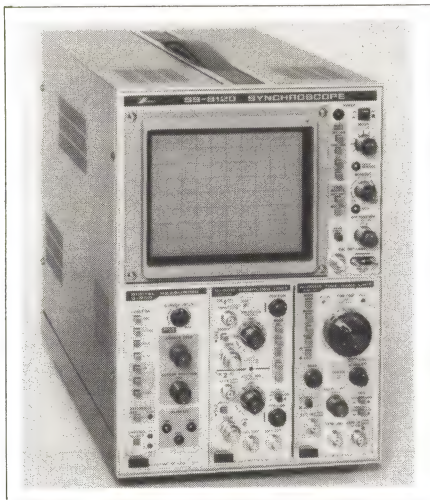
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NEW PRODUCTS: INSTRUMENTATION



MODULAR SCOPE

The SS-8120 accepts as many as three plug-in units, which can provide a 4-channel, 100-MHz oscilloscope; a 4-channel, 1-GHz sampling oscilloscope; a 2-channel digital oscilloscope; or a 2-channel ultrahigh-deflection oscilloscope. The mainframe features a 7-in. dome-mesh CRT and a character generator, so that data from the plug-in units can be displayed on the CRT. In addition, the scope has signal-output terminals for vertical signals, time-base signals, gate signals, and calibration voltages. It will accept the following plug-in units: the V810, a standard, dual-trace amplifier for dc to 100 MHz; the V811, a 10- μ V/div differential-input amplifier; the H-830 with two time bases (one for the main sweep and the other for the delayed sweep); the U-850 for displaying time and voltage data; the U-855 2-channel delay-line unit; and the V860 2-channel sampling unit. SS-8120 mainframe, \$4340; plug-in units, \$1440 to \$5545.

Iwatsu Instruments, 430 Commerce Rd, Carlstadt, NJ 07072. Phone (201) 935-5220.

Circle No 396

350-MHz SCOPE

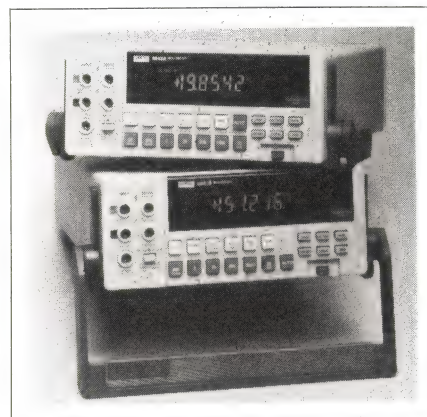
The PM 3295 analog oscilloscope features a 1-nsec rise time, a 4-div/nsec writing speed, full programmability with an IEEE remote-control option, cursor-referenced



measurements, and data readouts on its CRT. The 350-MHz scope can automatically set amplitude, time base, trigger function, and display position; it retrieves off-screen traces quickly. The scope doesn't have dial settings on the instrument panel; instead, it presents status indications on LCDs and LEDs. It displays as many as four waveforms. Specifications include a 1-mV/div to 5V/div sensitivity and 50 Ω /1-M Ω input impedance. \$5150; without screen readouts, \$4750. Delivery, eight to 10 weeks ARO.

Philips Test & Measuring Instruments Inc., 85 McKee Dr, Mahwah, NJ 07430. Phone (201) 529-3800.

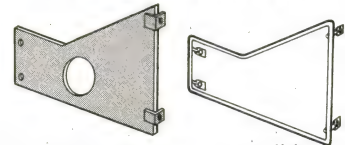
Circle No 397



5½-DIGIT DMM

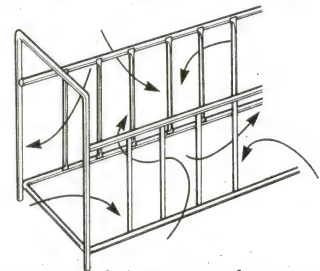
Offering 0.003% basic dc accuracy and 0.08% basic ac accuracy (1-year interval), the 8842A multimeter provides 100-nV resolution for dc-voltage measurements, 1- μ A resolution for dc-current measurements, and 100- μ Ω resolution for resistance measurements. Options include an IEEE-488 interface and true-rms ac measurement. Three rack-mount

How to design for ...weight reduction



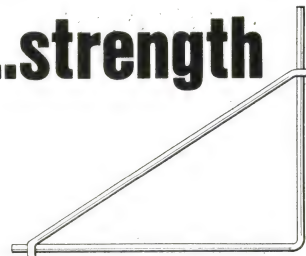
Do not use unnecessary solid surfaces. Substituting welded wire reduced the weight of this end bracket 35% over original sheet metal part. Pound for pound steel wire costs no more than other metals. And because less material is used, the savings are always significant.

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Leave plenty of open area for easy cooling. By putting metal only where needed, welded wire assemblies improve air flow and heat dissipation.

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CIRCLE NO 169

kits are available (for single- or dual-meter applications); one of these three kits will work with any system. The multimeter has a 2-year calibration cycle. \$995; IEEE-488 option, \$150; true-rms ac option, \$250.

John Fluke Mfg Co Inc, Box C9090, Everett, WA 98206. Phone (206) 347-6100. TWX 910-445-2943.

Circle No 398

LOW-COST GENERATOR

The Model 6200A program-mable-function generator offers rapid parameter setup, digital control of waveform symmetry, a burst mode, a high-resolution LED digital display, and a full IEEE-488 interface for all modes and parameters. You can store as many as 10 programs in battery-backed nonvolatile RAM. Spanning 2 mHz to 20 MHz, the device generates continuously variable, low-distortion sine-wave



signals; linear triangle waveforms and ramps; and minimal-aberration square waves and pulses (positive and negative). In addition, the unit accepts trigger and gate inputs. The burst mode generates a predetermined number (two to 500,000) of output waveforms. Square-wave and pulse rise and fall times are less than 12 nsec from 10 to 90% points. The generator includes automatic sweep of the output-waveform frequencies. You can set up/down sweeping of frequency between selected end points over a 10-decade range with sweep continuously ad-

justable over a 20-msec to 1000-sec/decade range. A VCO permits a 1000:1 frequency change. Option 20, an external-signal phase-lock and counter option, adds crystal control for frequency stability. Drift is less than ± 20 ppm over the 0 to 40°C range. The unit measures 5.5x11.8x13.6 in. and weighs 11 lbs. \$1995; Option 20, \$395.

Ballantine Laboratories Inc, Box 97, Boonton, NJ 07005. Phone (201) 335-0900.

Circle No 399

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Dice Series emulators feature real-time tracing. Eight-bit units come with a 64k-byte memory capacity; 16-bit emulators come with 128k bytes of memory, expandable to 384k bytes. The devices feature breakpoint and logic-analyzer capability (an oscilloscope is required for a timing-waveform display). They connect to target computers via two

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AD7549 NEW Model AD7549

Description Dual 12-bit Monolithic Multiplying DAC
Output Current
Package 20-pin, 0.3" narrow DIP

AD7225 NEW Model AD7225

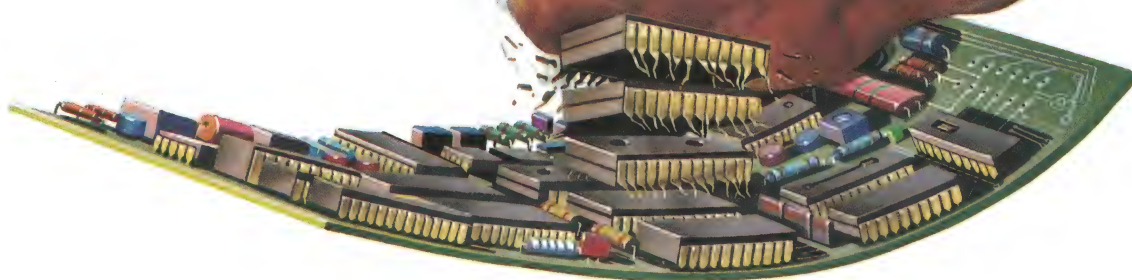
Description Quad 8-bit CMOS DAC with Output Amplifiers, Separate Reference Inputs for multiplying applications. Double Buffered Latch Structure for Simultaneous Update
Output Voltage
Package 24-pin, 0.3" narrow DIP

AD7528 Model AD7528

Description Dual 8-bit Monolithic Multiplying DAC
Output Current
Package 20-pin, 0.3" narrow DIP

AD7226 Model AD7226

Description Quad 8-bit CMOS DAC with Output Amplifiers, common reference input for all four DACs
Output Voltage
Package 20-pin, 0.3" narrow DIP



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Analog Devices, Inc., Two Technology Way, Norwood, MA 02062-0280; Headquarters: (617) 329-4700; California: (714) 641-9391, (619) 268-4621, (408) 947-0633; Colorado: (303) 590-8906; Illinois: (312) 653-5000; Maryland: (301) 992-1994; New York: (716) 425-4101, (315) 437-5277; Ohio: (614) 764-8795; Pennsylvania: (215) 643-7790; Texas: (214) 231-5094, (713) 664-6704; Washington: (206) 251-9550; Belgium: (3) 237 48 03; Denmark: (2) 845800; France: (1) 687-34-11; Holland: (1620) 81500; Israel: (052) 28995; Italy: (2) 6883831, (2) 6883832, (2) 6883833; Japan: (3) 263-6826; Sweden: (8) 282740; Switzerland: (22) 31 57 60; United Kingdom: (01) 9410466; West Germany: (89) 570050

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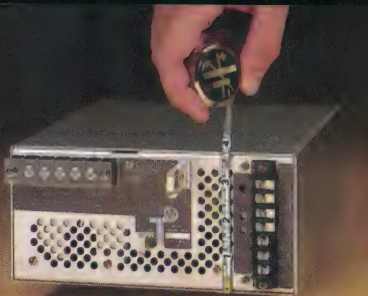
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national's text editor, Side Kick; IBM's PC Paint and PC-DOS; and AST's Six Pack support package. \$19,500, including a set of reference manuals.

Adaptec Inc., 580 Cottonwood Dr., Milpitas, CA 95035. Phone (408) 946-8600.

Circle No 401

RS-232C ports, one of which has automatic baud-rate selection. The units allow the operator to reference memory address, memory data, and I/O ports with symbols from the source code's symbol table. The series works with the following μ Ps: the Z80, 8085, 8048 family, 8086/88, 68000 family, 6502/65C02, and 6809/E. Prices range from \$4595 for Z80 and 8085 models to \$7795 for 68000 models.

Dux, 1850 E 17th St, Santa Ana, CA 92701. Phone (800) 233-9211; in CA, (714) 834-9211.

Circle No 400



CURRENT SOURCE

You can measure contact resistance with the Model 930 current source and the Model 296HP mounting-kit combination. The kit consists of a pc board, a connector, a current-ad-

Here's the new flush mounted terminal strip...

This new plug-in terminal strip from BUCHANAN offers captive screw terminations in a high density package. The quick disconnect feature not only permits rapid board replacement but also assures proper reconnection, thus eliminating the tedious, error prone operation associated with barrier strips.

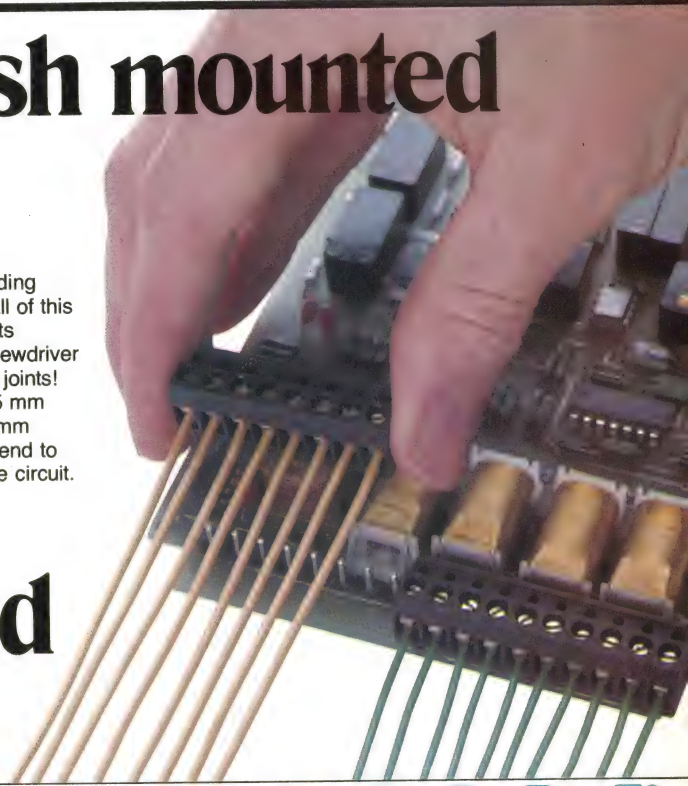
This versatile little connector packs over 11 terminations into a square inch of board space. Though small in size, its ratings are impressive; 14 AWG with strand protection,

13 amps and up to 300 volts depending upon pin spacing and application. All of this in a safe, dead-front design that rests directly on the PC board so that screwdriver force is not passed on to the solder joints!

Available today in 27 sizes ... 5 mm centerlines from 2 to 20 circuits; 10mm centerlines 2 to 10 circuits ... plus end to end mounting without losing a single circuit.

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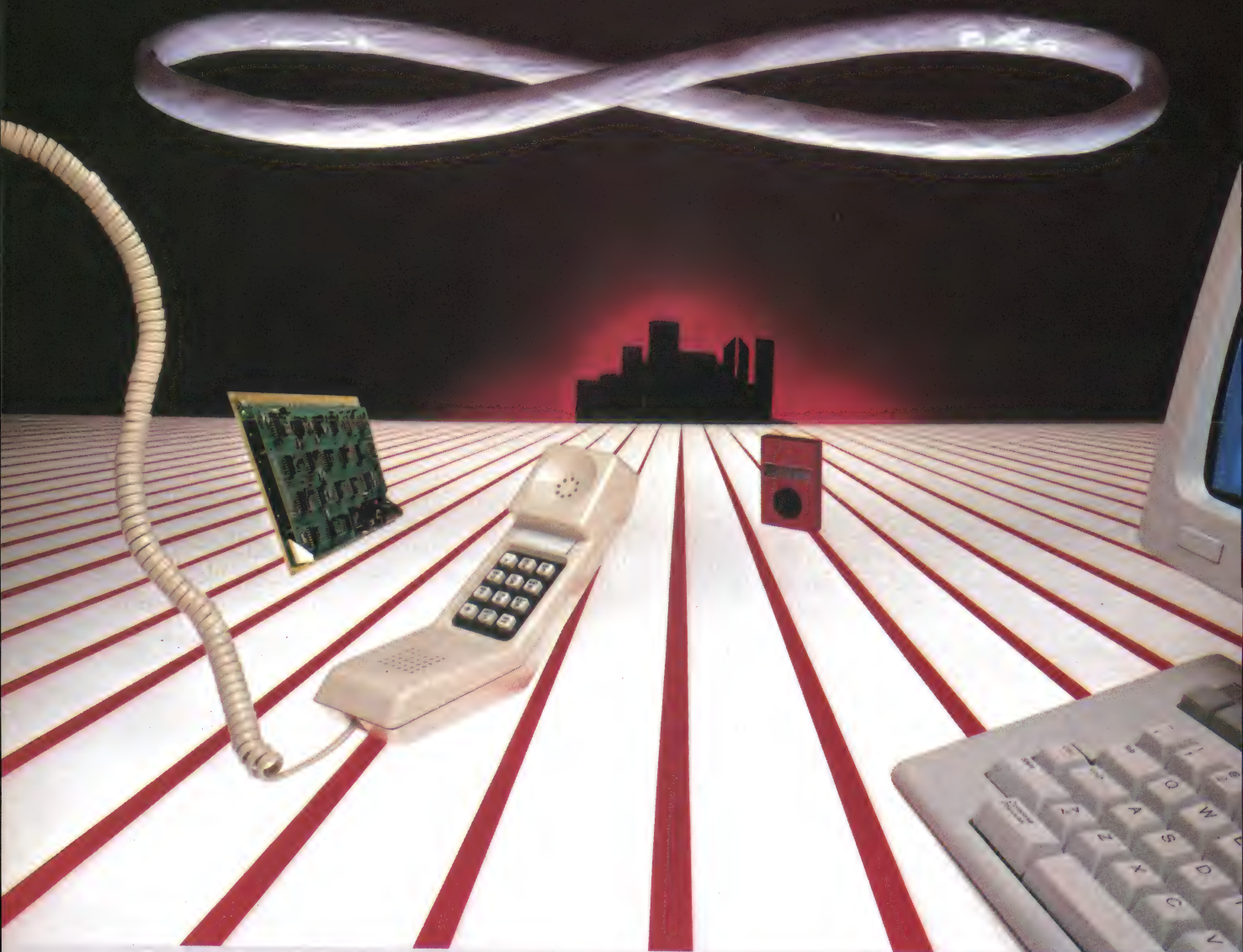
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justment potentiometer, a power transistor, and other components, and it provides as much as 0.5A of constant current. The 930/MK296HP output adjusts from 0.005A to 0.5A. Isolation from the power source is 50 μ A/V, current load regulation is 0.005% max, and temperature stability is $\pm 0.01\%$ /°C. You can parallel assemblies to achieve outputs of 1A or higher. Each assembly measures 3.2 x 4 x 1.25 in. \$156.

Calex Mfg Co Inc, 3355 Vincent Rd, Pleasant Hill, CA 94523. Phone (415) 932-3911. TLX 338506.

Circle No 402

DISK ANALYZER

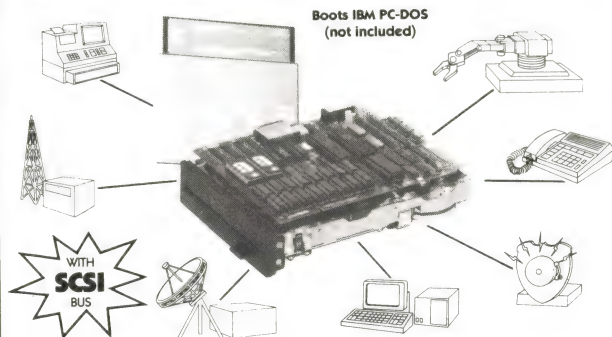
The DJ disk-drive analyzer offers graphics to speed the testing of floppy-disk drives, and it performs a full set of analog and digital tests. Real-time displays for such tests as radial head alignment, index-pulse timing, and rotation speed let untrained technicians adjust drives. An operator needs only three front-panel controls—test, restart, and print—to run a full analysis with hard-copy results. The analyzer also offers as an option complete annotation of amplitude, timing, lobe ratios, and read/write errors. For the window-margin test, the unit calculates and displays a probability-density function as well as code number and margin time. You can set test sequences and pass/fail limits via the keyboard and then store them on an EEPROM cartridge, which is removable to accommodate the testing of various manufacturers' drives. The analyzer, including probes and a choice of one power cable, one interface cable, and one alignment diskette, costs \$8500; test cartridge, \$100.

Nicolet, Oscilloscope Div, 5225 Verona Rd, Madison, WI 53711. Phone (608) 273-5008.

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Sysoft SA
6926 Montagnola
Switzerland
Tel 091 54 31 95
Telex 79 671 syst ch

CIRCLE NO 177

NEW PRODUCTS: INTERNATIONAL

VOLTAGE REFERENCES

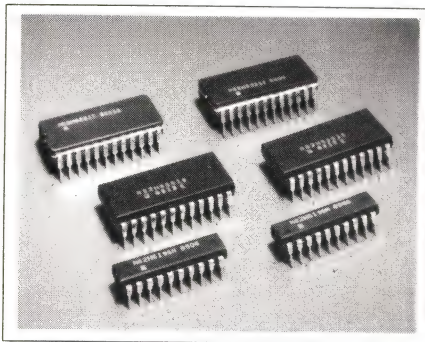
The REF25Z and REF25 low-power voltage references are housed in TO-92 plastic packages and TO-18 cans, respectively. The REF25F provides a nominal output voltage of 2.5V; its reference voltage has a tolerance of $\pm 2\%$ and a typical temperature coefficient of 35 ppm/ $^{\circ}\text{C}$ (maximum 70 ppm/ $^{\circ}\text{C}$) over a 0 to 70 $^{\circ}\text{C}$ temperature range. The device requires a minimum operating current of 60 μA . It also requires only a single external resistor for operation. The REF25 has a voltage tolerance of $\pm 1\%$ and a typical temperature coefficient of 25 ppm/ $^{\circ}\text{C}$. The REF25Z costs £0.27 (10,000).

Ferranti Electronics Ltd, Fields New Rd, Chadderton, Oldham, Lancashire OL9 8NP, UK. Phone 061-624 0515. TLX 668038.

Circle No 404

Ferranti Electric Inc, 87 Modular Ave, Commack, NY 11725. Phone (516) 543-0200.

Circle No 405



PROMs

Available with three access-time ratings, the 82HS195, 82HS321, and 82HS641 are field programmable, integrated fuse bipolar PROMs with capacities of 16k, 32k, and 64k bits, respectively. The 20-pin 82HS195 is organized as $4\text{k} \times 4$ bits and is available with access times of 25, 35, and 45 nsec max. Its power dissipation is typically 35 $\mu\text{W/bit}$. The 24-pin 82HS321 is organized as a $4\text{k} \times 8$ -bit device and is available in 30-, 35-, and 45-nsec maximum access-time versions; the 24-pin 82HS641 is or-

ganized as $8\text{k} \times 8$ bits and has access-time ratings of 35, 45, and 55 nsec max. Both the 82HS321 and 82HS641 dissipate 20 $\mu\text{W/bit}$ typ. On-chip address decoding, chip-enable inputs, and 3-state outputs enable you to use multiple devices for memory expansion. The PROMs are supplied with all outputs at a logical high. You can program them on commercially available PROM programmers. The devices are available in commercial or military temperature ranges and in plastic or ceramic DIPs and plastic leaded chip carrier packages. Approximate prices, depending on importing country, are \$11 for the 82HS195, \$20 for the 82HS321, and \$38 for the 82HS641 (10,000).

Philips, Elcoma Div, Box 523, 5600 AM Eindhoven, The Netherlands. Phone (040) 757005. TLX 51573.

Circle No 406

Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94086. Phone (408) 739-7700.

Circle No 407

LCD

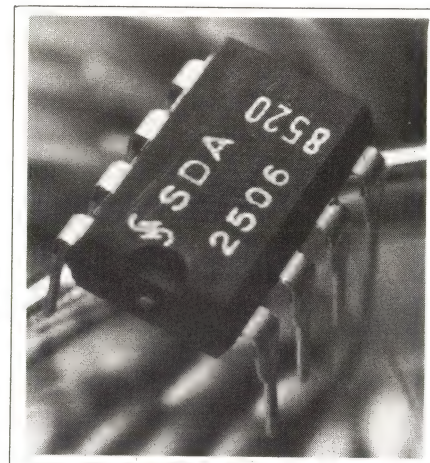
This 8-digit LCD incorporates 7-segment, $\frac{1}{2}$ -in.-high digits; eight decimal points; and three colons. Suitable for direct-drive systems where a wide viewing angle is critical, the LCD is compatible with most popular LCD driver ICs. It is supplied with integral bonded connector pins for pc-board mounting or with contact pads suitable for elastomeric connectors. Versions are available for -10 to +58 $^{\circ}\text{C}$ or -30 to +85 $^{\circ}\text{C}$ operating ranges. Transflective or reflective polarizers are also available. £8.50 to £10 (1000).

EEV Lucid, Waterhouse Lane, Chelmsford, Essex CM1 2QU, UK. Phone (0245) 261777. TLX 99103.

Circle No 408

EEV Inc, 7 Westchester Plaza, Elmsford, NY 10523. Phone (914) 592-6050.

Circle No 409



EEPROM

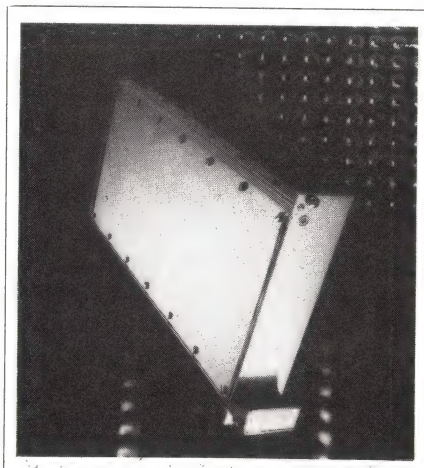
Housed in an 8-pin DIP and drawing <5 mA from its single 5V supply in all operating modes, the SDA2506 EEPROM provides 128×8 -bit non-volatile memory. Programming requires 10 msec per 8-bit location max. The 8-bit data transfers are performed bit-serially using an on-chip bidirectional shift register and three control lines. A protective circuit prevents accidental reprogramming. \$2.95 (1000).

Siemens AG, Zentralstelle für Information, Postfach 103, 8000 Munich 1, West Germany. Phone (089) 2340. TLX 5210025.

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Siemens Components Inc, 186 Wood Ave S, Iselin, NJ 08803. Phone (201) 321-4842.

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card modules allows you to place an RFI screen around individual Euro-cards within a rack. The module's guide rail incorporates a screening gasket and allows you to attach top and side covers, and the front and rear panels are closed off by a custom U-channel sealing strip. The sealing strips incorporate Monel metal to provide good electrical con-

tact with freedom from galvanic corrosion. For 1- and 10-MHz magnetic fields, the modules achieve 28- and 45-dB attenuation, respectively, and better than 66- and 87-dB attenuation, respectively, for electric fields at the same frequencies. Standard stock sizes include modules with dimensions of 3U×160 mm with 30.48-, 60.96-, or 106.68-mm

widths, 3U×220 mm with 30.48-mm width, and 6U×160 mm with 60.96- or 106.69-mm widths. From approximately £10.

Bicc-Vero Electronics Ltd, Flanders Rd, Hedge End, Southampton SO3 3LG, UK. Phone (04892) 81424. TLX 477984.

Circle No 412

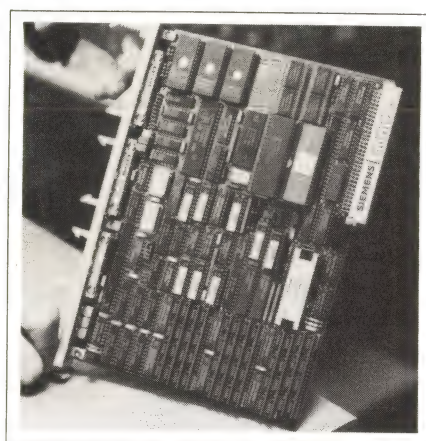
Bicc-Vero Electronics Inc, 40 Lindeman Dr, Trumbull, CT 06611. Phone (203) 372-0038.

Circle No 413



High Speed High Resolution Hard Copy Recorder

The Raytheon LSR-910M Line Scan Recorder with 8k memory capacity stores up to 2000 data elements per line. Simulates high speed printing for maximum data acquisition. Prints 16 shades of gray with a resolution of 150 data elements per inch. Accepts digital or analog input. Rugged design withstands shocks of 50g's for 11ms. For details, contact **Raytheon Ocean Systems Company**, Westminister Park, East Providence, RI 02914 USA Telephone (401) 438-1780 TELEX 6814078.



GRAPHICS BOARD

The AMS-M354 graphics board for AMS Bus systems provides 1024×1024-pixel resolution, an 8-color display, and a blink function. Running GKS (Graphics Kernel System), the board incorporates a GDC7220A graphics controller, supported by 384k bytes of refresh memory, an 8088 μ P, and an 8087 math coprocessor. You can operate the board with a 60-Hz refresh rate. The board's capabilities range from simple bar chart to high-definition CAD displays. DM 4900.

Siemens AG, Zentralstelle für Information, Postfach 103, 8000 Munich 1, West Germany. Phone (089) 2340. TLX 5210025.

Circle No 414

RS-232C LINK

This interface converter allows you to link RS-232C serially interfaced equipment to a parallel port such as the Centronics interface. An on-

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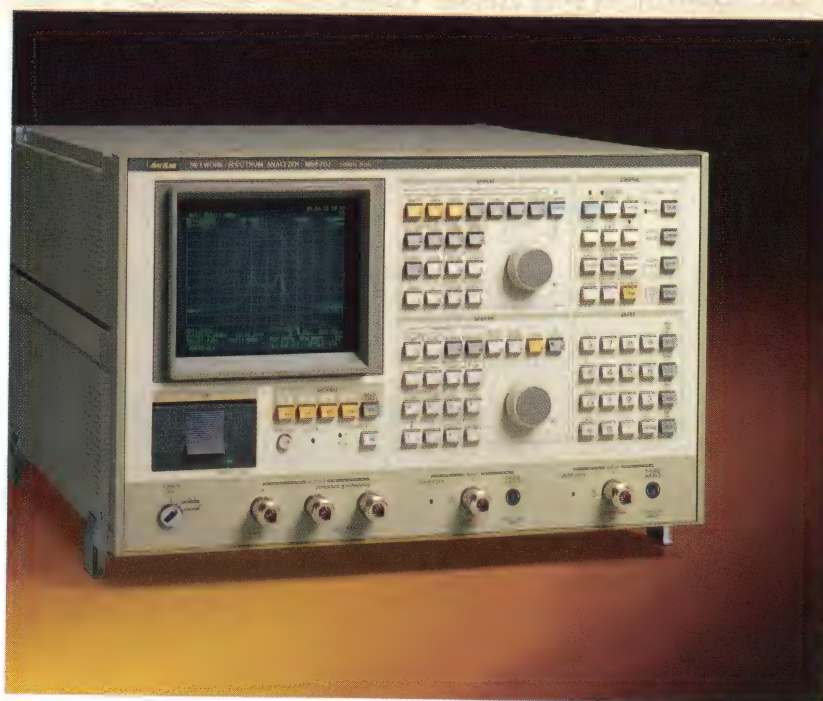
- Affordable – all the benefits of industry standard volume-produced equipment brought together in one integrated package.

- Available shortly: 8051, 80286, 68020

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MS620J Network/ Spectrum Analyzer

"Super-wide." That's the only way to describe the MS620J, which features a frequency range of 100kHz to 2GHz. Yet with its fully synthesized signal source and 0.1Hz step interval, it's super-precise, too. There's also a non-volatile memory for up to 10 different sets of data (key inputs, measured values, even corrected values).

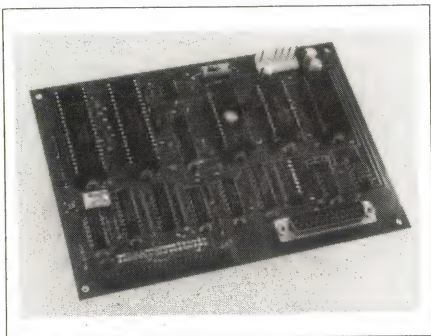
The MS620J handles network analysis, impedance analysis, and even spectrum analysis — and the screen displays sophisticated tools such as Smith and polar charts, too. A Personal Test Automation option puts fully

automatic operation at your command, without the need for a separate controller. And best of all, you can opt to see two — or more — different displays on the screen at the same time. Don't need quite *that* much range? Take a look at Anritsu's MS560J Network/Spectrum Analyzer, which covers the band from 100kHz to 300MHz. No matter which you choose, you'll find it ideal for testing transmission and impedance characteristics, noise, compression and expansion, distortion, spurious emissions, and more. But anything this super you'll want to see for yourself. So contact Anritsu today.

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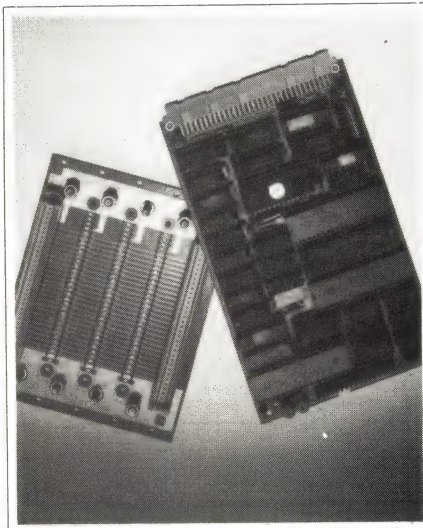
version, £175; low-power version, £198.

Systemation Developments Ltd,
Systemation House, Rowan Close,
Portslade, Brighton, E Sussex BN4
2PT, UK. Phone (0273) 423102.
TLX 87445.

Circle No 415

STE BUS BACKPLANES

Conforming to the IEEE P1000 STE Bus specification, these 5- and 10-slot backplanes use a multilayer pc-board construction and 0.5-mm track separation. This construction achieves a typical unloaded signal-line characteristic impedance of 60Ω. The backplanes are fitted with DIN 41612 connectors, with long connector pins and reverse-mounted bridging shrouds in the end positions, which allow you to mount space-saving plug-in termination networks. Prices for the 5-



and 10-slot backplanes are £70 and £107, respectively.

Dage (GB) Ltd, Eurosem Div,
Rabans Lane, Aylesbury, Bucks
HP19 3RG, UK. Phone (0296)
33200. TLX 83518.

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Digital Equipment Corp., 146 Main St., Maynard, MA 01754. Phone (800) 344-4825.

Circle No 417

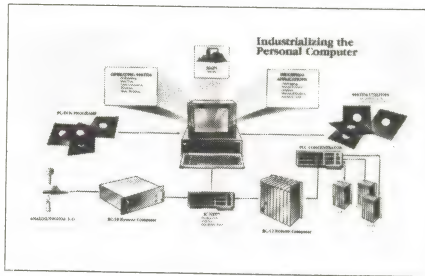
PC-TO-VAX LINK

The PCLink integrates the IBM PC or Apple Macintosh with minicomputers in the DEC VAX Series. A virtual disk capability allows multiple PCs to run such programs as Lotus 1-2-3 with transparent access to data stored on a host VAX. This function reduces the PC's disk requirements and permits centralized data control. Bidirectional binary and text-file transfers are accomplished via an RS-232C connection or through a modem. The company's proprietary error-correcting protocol adjusts packet sizes to provide maximum data throughput for a given line quality. With one command, you can define an arbitrary group of files to be transferred. For running VAX applications, the soft-

ware provides VT100, VT220, Adds Viewpoint 60, and Televideo 950 terminal emulation on the PC and the Macintosh. Licensing for the host side of the package ranges from \$2000 for five PCs to \$15,000 for an unlimited number of PCs on one host.

Pacer Software Inc., 100 Pennsylvania Ave, Suite 320, Framingham, MA 01701. Phone (617) 879-1765.

Circle No 418



MULTITASKING OS

IC-DOS is a real-time, multitasking operating system for use with 8088- and 80286-based computers, including the IBM PC/XT and PC/AT. It also runs on such industrial PC-bus computer systems as the IBM 7532 and the company's BC-10 and BC-12. It provides real-time, interrupt-driven architecture and the ability to assign as many as eight priorities to interrupts. A multitasking feature allows the computer to control several processes or run as many as 30 program tasks simultaneously; switching time between tasks is 200 μ sec. You can configure as many as 10 windows with adjustable sizes and screen locations. An optional distributed-file system, IC-NET, permits one host computer to control as many as 255 remote processes. Each node in the network is managed by a remote, hardened computer that controls and measures the process. Data is transmitted back to the host via the network at a rate of 1M bps. An optional PC-DOS emulation module allows you to run PC-DOS programs under IC-DOS as a task in a display window. Process information can then be used by such PC-DOS programs

as Lotus 1-2-3. From \$595.

Action Instruments Inc., 8601 Aero Dr, San Diego, CA 92123. Phone (619) 279-5726. TWX 910-335-2030.

Circle No 419

SOURCE-CODE EDITOR

AEdit-DOS, an editor for creating and editing source and object code and text, runs on IBM PCs and compatible systems under PC-DOS 3.0. It also runs on the company's Intellec Series III and IV development systems and the iRMX operating system. You select commands from a menu. Features include escape from DOS, hex-code entry, dual-file editing, split-screen windows, and a macro library. \$350.

Intel Corp., Literature Dept W-257, 3065 Bowers Ave, Santa Clara, CA 95051. Phone (503) 681-2279.

Circle No 420

PROGRAMM CONTROL

A control program for this company's EPROM multiprogrammer, Multiprogrammer Control Program (MCP), allows an IBM PC to issue commands to and control the operation of the multiprogrammer via an RS-232C interface. Because the MCP was written for disk-based operation, you can program and compare directly from files. You can also save the data stored in your master devices into binary files and then program directly from the files. \$195.

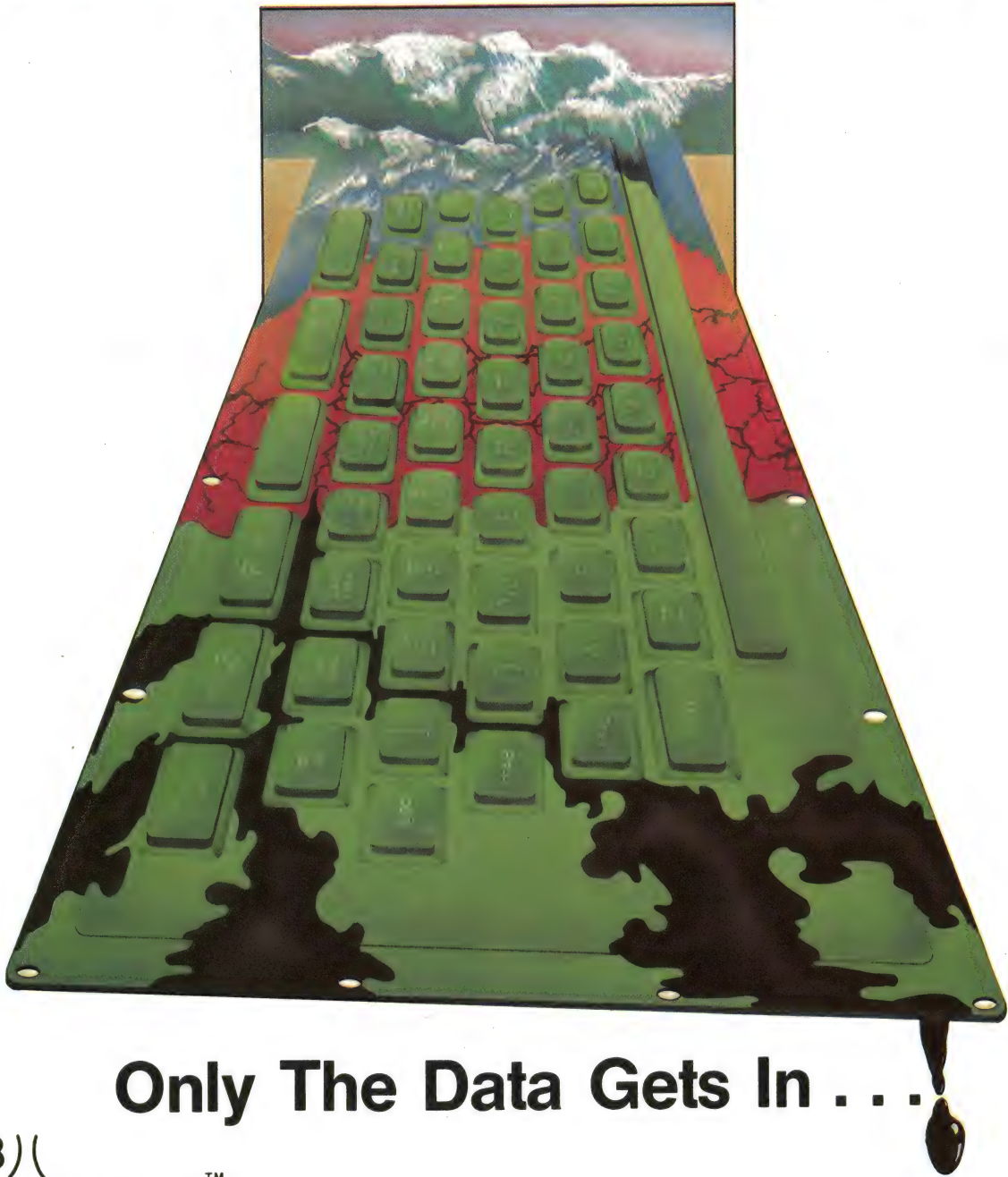
Bytek, Instrument Systems Div, 1021 S Rogers Circle, Boca Raton, FL 33431. Phone (305) 994-3520.

Circle No 421

KNOWLEDGE SYSTEM

M.1, version 2, is an IBM PC-based knowledge engineering tool written in C. According to the company, the program has a four- to fivefold performance improvement over the earlier version, which was written in Prolog. Version 2 increases the

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number of rules from 200 to more than 1000. By integrating this system with conventional software, you can provide end-user access to database files and numerical functions or add advisory capabilities to existing applications software such as spreadsheet programs. Running on an IBM PC, PC/XT, PC/AT, or compatible computer, the software allows you to develop knowledge systems that may be incorporated into end-user systems. Development system, \$5000; without development features, \$500.

Teknowledge Inc., 525 University Ave, Palo Alto, CA 94301. Phone (415) 327-6640.

Circle No 422

LIGHT-PEN DRIVER

Conductor 2.0 is a light-pen driver for use with Symphony 1.1 and Lotus 1-2-3. A submenu allows you to select any @ function with a light

pen; the function is automatically written into the formula. Two additional driver programs, Gemlight and Warpstar, enable the light pen to operate with Gem and Wordstar. With Gemlight, you can replace a mouse with a light pen; you select menus and icons by touching the light pen to the monitor. Warpstar speeds word-processing time by 50% over standard operation without a light pen, according to the company. Using the keyboard, you enter a document without stopping to make corrections, then pick up the light pen and edit the copy. Light pen with Controller software, \$199.99; Conductor 2.0, \$79.99; Warpstar and Gemlight, \$69.99 each.

Warp Speed Computer Products Inc., 5555 S Inglewood Blvd, Los Angeles, CA 90230. Phone (800) 874-4315; in CA, (800) 826-1563. TLX 4949554.

Circle No 423

NETWORK ANALYZER

PMS-II is a critical-path network analyzer and scheduling package that calculates the early and late start/finish dates, float time, and critical paths of large projects. Each network can have as many as 2750 activities; you can link these networks to accommodate project sizes limited only by disk space. The software provides menus, a project-management tutorial, schedule calculations, what-if analysis, and a highlighted critical path. Report-selection functions include base-line comparisons on reports, exception reporting, project diagrams, dependency reports, and audit trails. The package runs on microcomputers under PC-DOS, MS-DOS, or CP/M-86. \$1295.

North America Mica Inc., 5230 Carroll Canyon Rd, Suite 110, San Diego, CA 92121. Phone (619) 458-1327.

Circle No 424

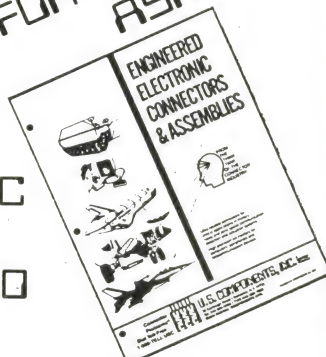
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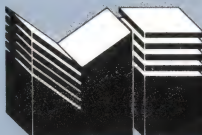
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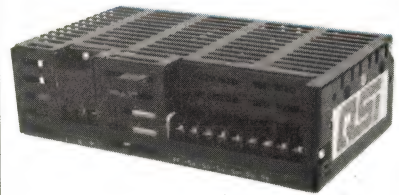
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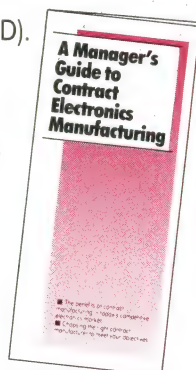
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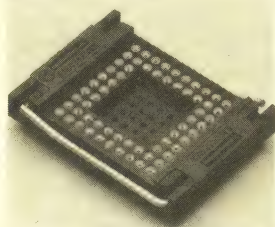
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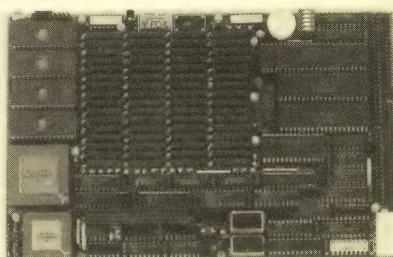
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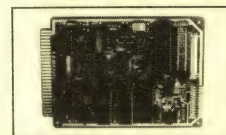
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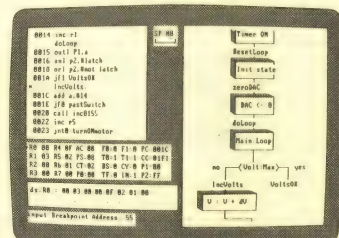
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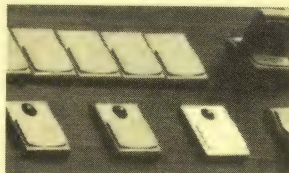
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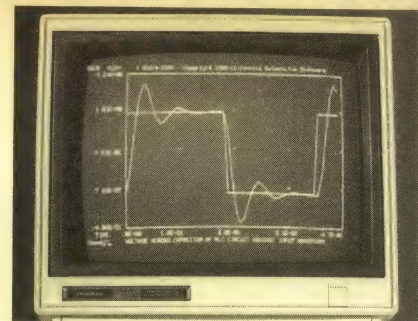
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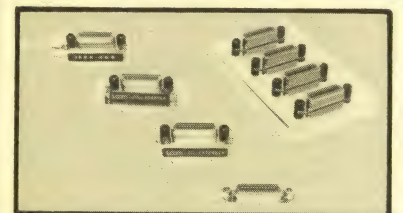
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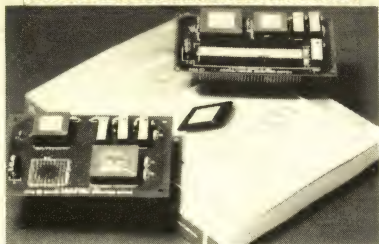
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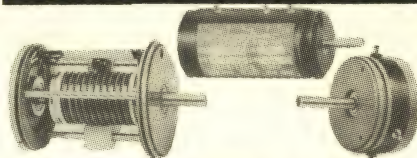
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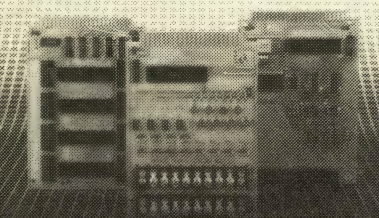


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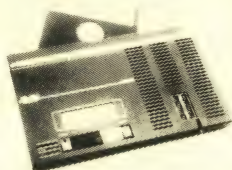
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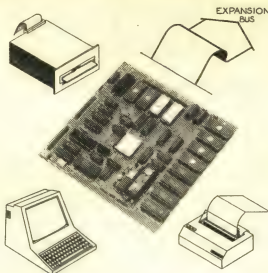


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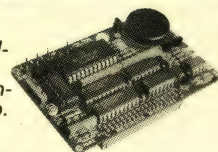
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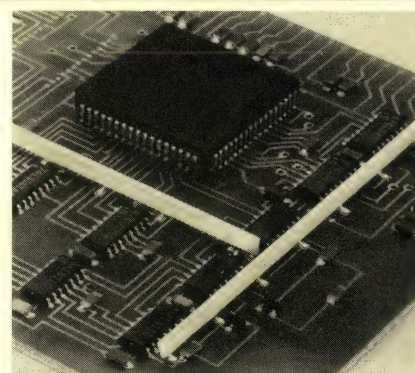
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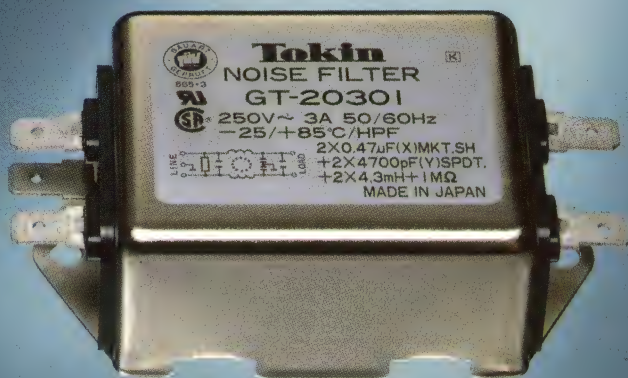
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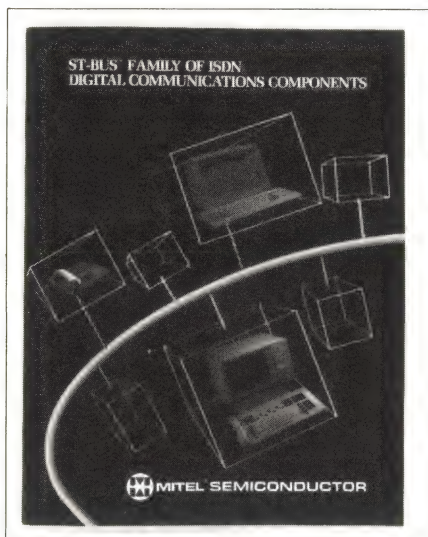
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Brochure features ISDN communications components

This 8-pg brochure introduces the manufacturer's communications components for the Integrated Services Digital Network (ISDN). The document describes switch and line-interface ICs as well as hybrids; it lists features, includes illustrations, and presents applications information. In addition, the brochure covers the Serial Telecom Bus (ST-Bus), a synchronous serial data bus for communication between components.

Mitel Semiconductor, Inquiry Management Systems, Box 911, Station U, Toronto, Ontario, Canada M8Z 9Z9.

Circle No 428

Thermal analysis explored

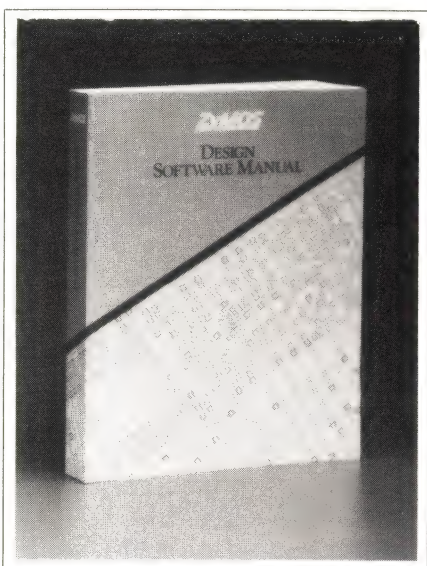
Reviewing applications of thermal analysis in the electronics industry, this 20-pg report describes state-of-the-art thermal-analysis techniques and shows how you can use the data derived from such analyses to characterize and evaluate electronic materials. Tables summarize the most commonly used techniques and their applications. The text details these applications, which include pc boards, encapsulants, and optical fibers. Among the remaining applications are insulating materials, solder, liquid crystals, and piezoelectric materials. Graphs plot ther-



mal-analyses results. Thermal-analysis instrumentation is covered.

Du Pont Co, Instrument Systems, Concord Plaza, Quillen Bldg, Wilmington, DE 19898.

Circle No 429

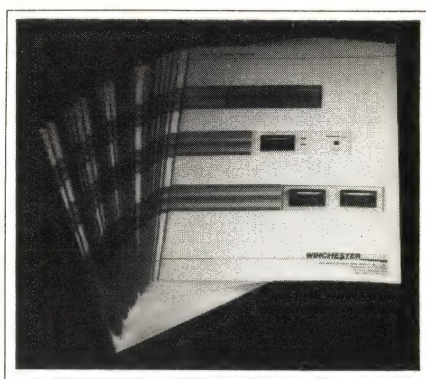


Manual offers user guides to software products

A comprehensive design-software manual suits both users and prospective users of the manufacturer's Zyp design system. The 760-pg book offers user guides on 10 of the manufacturer's Zyp software products. The book also includes reference manuals on four Zyp programs. You must request the book on company letterhead.

Zymos Corp, 477 N Mathilda Ave, Sunnyvale, CA 94086.

INQUIRE DIRECT



Winchester disk subsystems featured in catalog

Featuring more than a dozen models of fixed, fixed/removable, and removable Winchester disk subsystems, this 8-pg catalog is intended for those who use the manufacturer's Intellec Series II and III and Model 800 development systems. The models described spec 8M- to 72M-byte capacities. Among the options covered are a 256k-byte RAM print spooler and an iRMX-86 operating-system interface. The catalog provides applications information that helps users configure development systems and select options.

Winchester Systems, 400 W Cummings Park, Woburn, MA 01801.

Circle No 439

Catalog covers MOS products

Data sheets for more than 100 of the manufacturer's communications, memory, $\mu P/\mu C$, and consumer products comprise one section of *The 1985 MOS Products Catalog*. Another section focuses on the custom services that the company offers in the silicon-foundry, CAD/CAE-support, and gate-array and standard-cell areas. The catalog also lists more than 200 arrays and cells and provides information on development costs. In addition, it describes the company's methods for working with users of its application-specific ICs.

Gould AMI Semiconductors, Literature Dept, 3800 Homestead Rd, Santa Clara, CA 95051.

Circle No 440

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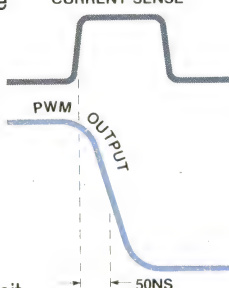
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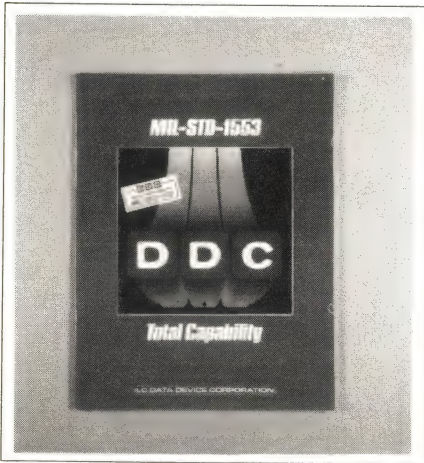
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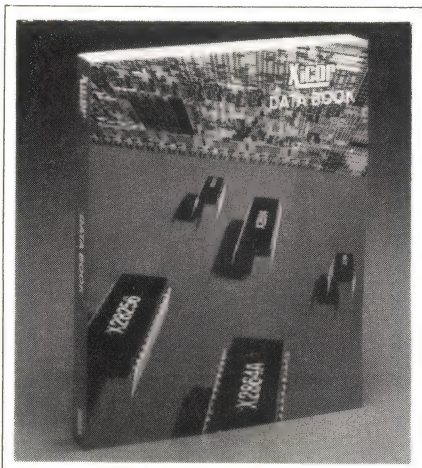


Brochure covers MIL-STD-1553 products

This 12-pg, 4-color brochure summarizes the company's products for the MIL-STD-1553 data bus. Among the products are bus controllers, remote terminal units, and bus monitors on industry-standard VME Bus, Unibus, and Multibus cards. Also presented are hybrid devices in 2x2-in. packages and building-block hybrids that let you produce any -1553 configuration. The manufacturer's test equipment, including a data-bus exerciser and a benchtop tester, are also covered.

ILC Data Devices Corp, 105 Wilbur Pl, Bohemia, NY 11716.

Circle No 441



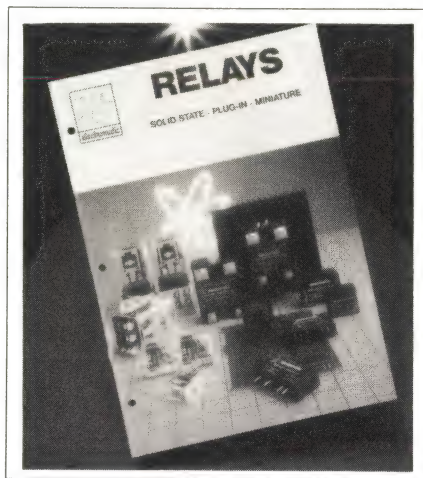
Data book characterizes nonvolatile-memory products

Covering nonvolatile memory products, this 464-pg data book describes the company's 17 series of

EEPROMs, six series of serial I/O devices, 11 series of nonvolatile RAMs, and the E²POT device. The book includes information on truth tables and read, write, and store cycles. It provides pin-configuration and functional diagrams and describes the functions of the pin terminals. The book also contains sections on applications, reliability, and packaging.

Xicor Inc, 851 Buckeye Ct, Milpitas, CA 95035.

Circle No 442



Relays and sockets featured in brochure

This 8-pg brochure features the manufacturer's line of solid-state, mechanical plug-in, and miniature pc-mount relays. The publication covers relays for horizontal and vertical pc-board or plug-in mounting, as well as snap-mount spade and octal-relay sockets. It lists the benefits of each type of relay and provides a relay-selection guide. Technical data is presented in tables, graphs, and diagrams.

Electromatic Controls Corp, 2495 Pembroke Ave, Hoffman Estates, IL 60195.

Circle No 443

Catalog details keyboards

This 40-pg keyboard catalog features the manufacturer's line of dome and wiping-contact keyboards and keyboard modules. The full-col-



or catalog provides engineering drawings, product specifications, and prices, along with keyboard features and legend options. Products covered include low-profile keyboards and stackable modules in several keypad styles. The keypads can be lighted, or they come with graphic-overlay legends and printed or molded-in legends.

Grayhill Inc, 561 Hillgrove Ave, La Grange, IL 60525.

Circle No 444

Linear and data-conversion products described

This company's fall 1985 product selection guide gives an overview of linear and data-conversion products. The 12-pg booklet lists key specifications for CMOS D/A converters, op amps, instrumentation amplifiers, voltage follower/buffers and comparators, and matched transistor pairs. Also detailed are voltage references, analog switches/multiplexers, sample/hold amplifiers, and serial data repeaters.

Precision Monolithics Inc, Literature Dept, 1503 Arbuckle Ct, Santa Clara, CA 95054.

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NEW BOOKS

The Raster Graphics Handbook. 345 pgs; \$37.50; Conrac Division and Van Nostrand Reinhold Co, New York, NY, 1985.

This handbook presents a comprehensive explanation of the hardware, software, and operating principles behind the computer-graphics industry. It also provides the criteria you need for selecting display devices. The book discusses display technologies and their modes of operation, graphic-controller design and principles, software and interface standards, and computer peripherals.

Inside the IBM PC AT, by T J Byers. 309 pgs; \$19.95; Micro Text/McGraw-Hill, New York, NY, 1985.

A practical guide for first-time and advanced users of microcomputers, this book shows how the PC/AT combines the resources of minicomputers and mainframe computers at the personal-computer level. Special

features discussed include enhanced graphics, extended interface options, networking, and high-density floppy- and hard-disk drives, with emphasis on the multi-user/multitasking environments.

For the novice, Byers provides illustrations and thorough descriptions; for the advanced user, the author examines the differences and enhancements in the AT's operating systems in comparison with other personal computers. For the computer professional, the book offers methods for adapting the PC/AT to custom applications.

Programming the IBM PC User Interface, by Henry Simpson. 228 pgs; \$18.95; Byte Books/McGraw-Hill, New York, NY, 1985.

This book presents a systematic approach to designing and developing programs for IBM PCs and compatible computers. The manual pro-

vides examples of programs in Basic that you can adapt for use with such languages as Pascal, C, and Forth. Simpson emphasizes programs that are easy for computer operators to learn and use. He explains how to use help menus for program control and how to design them and link them together into networks.

The work also covers such topics as the 12 design principles that help create easy-to-use programs; display formatting; the presentation of information; creating data-input screens; and the prevention of programming and operator errors.

Kalman Filtering: Theory and Applications, edited by Harold W Sorenson. 464 pgs; \$58.95 (\$35.35 for IEEE members); IEEE Press, Washington, DC, 1985.

This volume contains 45 reprinted articles explaining state-of-the-art applications and the fundamental theories of Kalman filtering. Applications covered in this volume focus on such areas as orbit determination, phased-array radar tracking, and power-station control systems. Included with the application and theoretical papers are tutorials that emphasize the major points of the reprinted papers.

Real-Time Microprocessor Systems, by Stephen Savitzky. 338 pgs; \$47.50; Van Nostrand Reinhold Co, New York, NY, 1985.

This book teaches design and implementation principles and techniques for microprocessor-based real-time systems. The emphasis is on practical advice, not theory. It's divided into three parts. Part 1 introduces the general concepts of real-time systems and serves as an introduction to the terminology of the field. Part 2 describes the design and implementation process, with emphasis on the techniques useful for real-time applications. Part 3 examines specific system organizations and their appropriate implementations.



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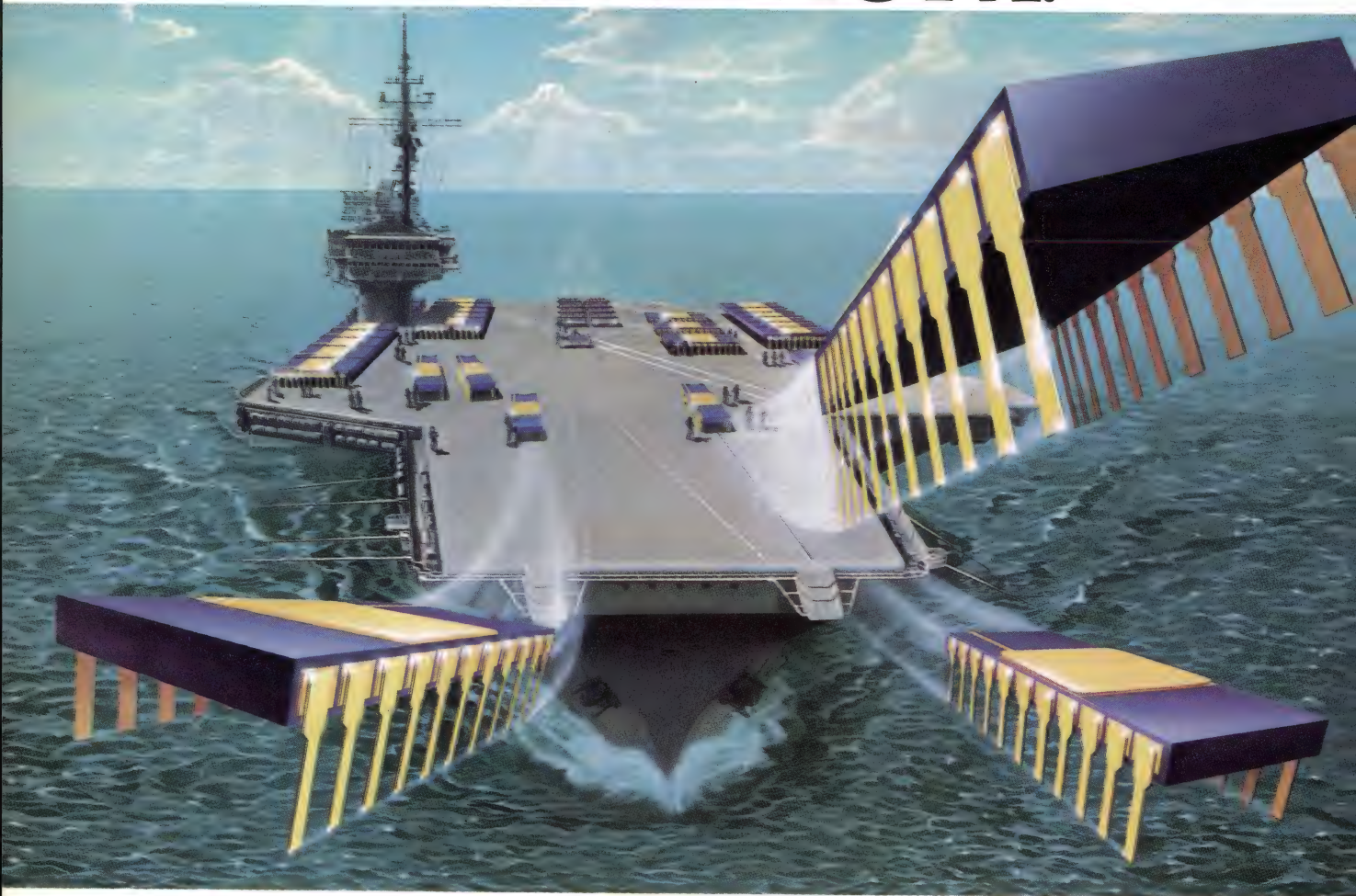
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PROFESSIONAL ISSUES

Company compensation strategies seek the right mix of salary and incentive

Deborah Asbrand, *Staff Editor*

Changing attitudes about employees' roles within their companies are leading employers to revamp the benefit packages they've traditionally offered their workers. Now companies are putting together compensation plans that mix annual salary and traditional benefits with performance incentives. Small, progressive electronics companies have led the way in innovative compensation plans and have started a trend that many larger companies have been compelled to follow. The result is a variety of compensation packages that give engineers and other workers a stake in the company's profits.

Though such plans are now often available to all workers in the companies that adopt them, the electronics industry's competition for engineering talent has been the principal inspiration for innovative compensation programs. "Two of the critical groups [that high-tech companies] look at are programmers and engineers," says Don York, executive vice president of Radford and Associates, a Santa Clara, CA, compensation consulting firm. "These people tend to be more mobile, and they're the ones who get snatched up by competitors or start-ups. We're finding that companies will have base-salary and merit-increase programs [for all employees], but they'll have something different for their engineers and programmers. They tend to be treated somewhat differently because they're such a key group to the organization."

As many smaller engineering-based companies are establishing programs that offer profit sharing, stock options, stock-purchase plans,



Michael McLaughlin

and cash bonuses in order to keep their technical specialists, so are more and more companies of all sizes and in all industry sectors turning to such incentives. Larger companies that once relied on competitive salaries and annual cost-of-living raises to attract workers are warming to the idea of additional cash compensation. In 1980, employees at 19% of medium- and large-size companies surveyed by the Bureau of Labor Statistics were receiving profit-sharing checks; by 1984, the figure had risen to 24%.

The growing popularity of incentive programs is having a snowball effect. As more companies elect to set up such programs for their employees, others are compelled to do the same to remain competitive in the labor market. As York observes, one reason companies are creating such programs is simply "because everyone else is doing it."

"Competition in most markets has heated up and become ferocious," says Alan Johnson, a principal with the compensation consulting firm Sibson & Co of Princeton, NJ. "A lot of companies are much more

concerned about survival and performance than they ever were before. It's much tougher now than it was five years ago to make a profit and stay up on the technological curve."

Compensation consultants also say that business realities are forcing companies to rethink their traditional compensation strategies and to come up with new solutions that inspire employees to do their best work by rewarding those who excel. As corporate survival becomes more difficult, managers are willing to pursue any avenue that promises to keep their businesses healthy and ahead of their competition, says Johnson. The result is incentive programs keyed to performance.

Attraction, retention, motivation

The key ideas of incentive programs, says York, are attraction, retention, and motivation of employees. "Companies can only do so much in these areas with their base-salary programs and benefits. That means you have to have a focus on stock participation and incentive compensation."

PROFESSIONAL ISSUES

These market changes are adding a new dimension to employee/employer relationships. "Many companies view their roles differently than they did 20 years ago in terms of employees," says Johnson. "Companies now look at employees as a valuable resource that should be treated well." Johnson adds that, though the fruits of such changes can be additional financial rewards for employees, the changes also mean employee performance is coming under greater scrutiny. "Companies are much more realistic about performance and what it means. Throughout American industry there's a much greater emphasis on performance, not only the company's, but the individual's."

Employees' attitudes have changed along with those of their employers. The era of the one-company career is long past, and employees, particularly those in the high-technology and electronics industries, are now drawn to jobs that provide more than steady work and salary. They want a challenge to their work and a feeling that their work is essential to the company's pursuits.

The problem of maintaining a consistent technical team, as well as keeping its members motivated, has a different character at a large company than at a small concern. The larger companies usually offer higher base salaries than smaller companies, but the worker is more likely to feel a distance between his or her work and the company's broader goals and activities. To combat such feelings of detachment, Texas Instruments provides its 80,000 employees with a compensation package that includes annual bonus incentives and a stock-purchase plan.

Under the terms of the stock-purchase plan, all employees are entitled to purchase company stock. The amount of stock employees have the option to purchase is based on their annual salary. Payment for the

stock is deducted from their salaries over a 12-month period, during which time the company pays interest on the amount deducted. When the payments have been completed, employees have another 12 months to decide whether they want to exercise their option to buy the stock. If they decide not to purchase the



stock, their money is refunded along with the interest earned. More than 50% of the company's US employees elected to purchase stock in 1985.

Large, established companies must also respond imaginatively to the attractions of small start-ups. When nearby start-up companies in the early 1980s began luring away large numbers of its engineering staff, the management of Tektronix Corp (Beaverton, OR) took steps to maintain the company as a viable alternative for engineers. Tektronix has long had profit-sharing; 35% of the company's worldwide profits are distributed among all employees. It also maintains a stock-option program that approximately 10% of the company's employees are invited to participate in annually. Engineers account for a large number of the employees who receive the stock option, says David Franks, strategic compensation programs administrator for Tektronix.

The real weapon in Tektronix's arsenal, however, is its innovative Strategic Program Units (SPUs). These programs provide engineers with an unusual opportunity to increase their stake in the profits earned from a product on which they have worked.

Tektronix designed its SPUs to give employees the opportunity to pursue the development of products not applicable to the company's existing product lines. Once a project is approved, a core group of 10 to 12 individuals is offered the option of being assigned to the project full time. The SPUs carry with them a special incentive program that makes the offer especially attractive. Employees who work on the long-term development of a product are entitled to a percentage of excess profits once the product has been marketed. In some instances, says Franks, the incentive payment, typically covering a period of three to five years, can amount to twice the participant's annual salary.

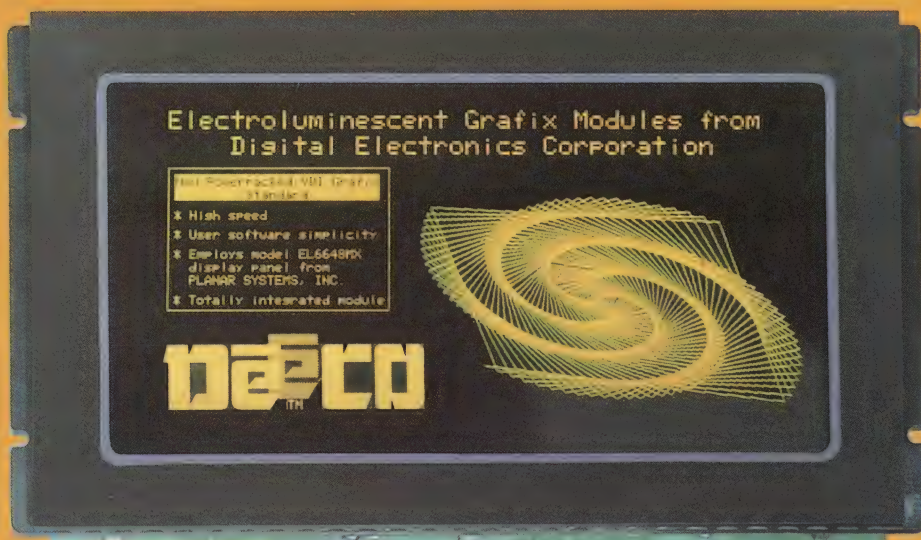
Structured to resemble the atmosphere of a start-up company, the SPU arrangement entails similar financial risks. Employees who choose to work on the projects receive the incentive of a potentially lucrative, long-term payment should the product be a success, but they are required to forego their profit-sharing checks while working on the project.

Small companies need a boost

Though they often present an attractive employment alternative, small companies are frequently at a disadvantage in the stiff competition for engineers. A 1985 federal report, *The State of Small Business: Report of the President*, expressed concern over the plight of small-business owners in the high-technology sector, where small companies compete for technical professionals with large, established concerns that are able to offer more gainful salaries.

Incentive programs are thus even more vital to these small, young companies, where knowledgeable, skilled employees are often the businesses' most valuable asset. A 1982 study conducted for the Small Business Administration by a Virginia consulting firm, James Bell and As-

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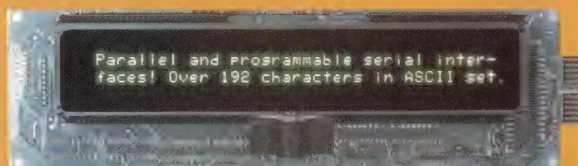
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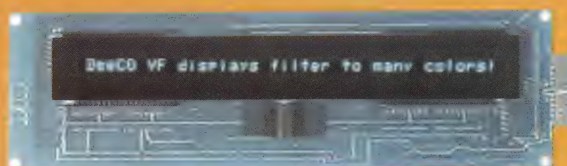
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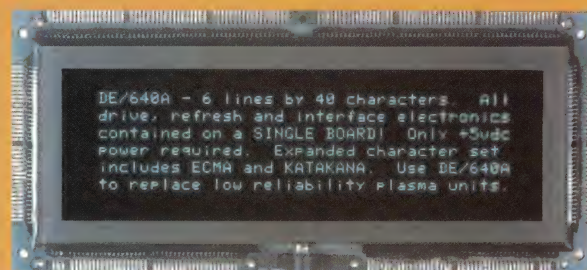
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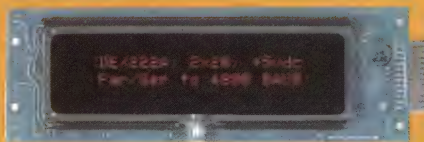
Vacuum Fluorescent Text Module allows 80 characters to be displayed. Only +5 vdc power needed. Same features as display below.



Vacuum Fluorescent Text Module, 40 characters. Same form factor as 2 lines x 40 characters display at left. RS-232 voltage levels optional on all VF display modules.



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Vacuum Fluorescent Module, super fast bit mapped display. 256 x 64 pixels.

PROFESSIONAL ISSUES

sociates, found profit-sharing plans common in small businesses. Fifty-six percent of surveyed companies having 25 to 99 employees offered profit sharing, and 65% of those companies with fewer than 25 employees offered the benefit.

Incentive programs' popularity with small start-up companies is a matter of economics. Young companies frequently operate on shoe-string budgets, so offering equity is a pragmatic and affordable way of attracting new employees. Employees' base salaries are a fixed cost. Incentive compensation, on the other hand, obliges a company to pay only if it becomes profitable. "It's an attempt to convert what is a fixed expense into a much more variable expense, and that's very attractive to a small start-up," says Eric Marquardt, a principal in the San Francisco, CA, office of Wyatt Co, a compensation consulting firm.

"Few companies try to offset the risk of working in a start-up with aggressive compensation packages," says Marquardt. "They typically can't afford it. That's why the opportunity for equity ownership and the high leverage you get from having stock in a start-up company are the only effective ways these companies are able to attract people in the beginning."

At Pacific Monolithics, a Sunnyvale, CA, maker of gallium arsenide monolithic microwave ICs, each of the company's 40 employees is a stockholder, "right down to the janitor," says Allen Podell, senior vice president for technology development and one of the company's four founders. Podell and his colleagues started the company in early 1984. Podell, a former engineer, envisions employees retaining 30% ownership in the business. "I want everyone to feel a part of it," he says.

Opportunity and reward for individual contribution are what Eric Wilson, Pacific Monolithics' manager for business development, sees as two important pluses of working

for a start-up company. As an industry engineer, Wilson says he was frustrated by a limiting role that prevented him from contributing "even a decimal point to the annual report." For Wilson, seeing a direct tie between his contributions and rewards is important. "I don't think people join a company because of

Work incentives are a boon to many employees, allowing them to see a cause-and-effect relationship in their work that makes their jobs more satisfying.

the money waved in front of them," he says. "I think people join a company because they see they'll be rewarded in proportion to what they contribute."

Fazal Ali joined Pacific Monolithics as a design engineer last June. Working for a small company allows him to see the end results of his circuit designs, and that, he says, "makes a world of difference." At Pacific Monolithics, he feels he's part of the company, a feeling he says was missing from his previous job at a large company. As part owner of Pacific Monolithics, Ali says he finds greater satisfaction in his work and often puts in 60 hours each week. "Here, I'm part of the team. I own part of the company, so I have to work hard, develop good products, and make money for the company."

Plan programs with care

Work incentives are a boon to many employees, allowing them to see a cause-and-effect relationship in their work that makes their jobs more satisfying. But financial compensation can be a risk, and it can hurt people where they feel it most—their wallets. "The potential downside in stock participation is

that you get all this stock as a reward for your efforts, and the market value of the stock goes down," says York. Bonus incentives offered to some employees and not others can also cause problems.

Companies' attempts to set up incentive compensation can stumble if they fail to understand that setting up the program is a 2-step process. Once a company commits itself to incentive and reward plans, it must also take on the sometimes greater task of revamping its employee-evaluation process. Establishing a fair assessment process, the terms of which are agreeable to both management and employees, is key to any program's success.

Companies may also find their compensation programs in trouble if they go too far in trying to measure performance. Not every aspect of a job can be held up for measure, warns Johnson. Engineering work is particularly difficult to measure. "It's very difficult to come up with a quantitative measure of engineering performance," says Johnson. "If you tell an engineer to produce 12 designs in one year, then he'll produce 12 designs. They may not be very good designs, but they will have met the goals."

"Many companies look at pay for performance as a panacea," says Johnson. They see the programs as a solution to their inability to face up to employee performance problems and to reward good performance, as well as their inability to communicate with employees, he says. The important aspect of setting goals is not the goals themselves, says Johnson, but the dialog and the agreement about what the employees should be doing. **EDN**

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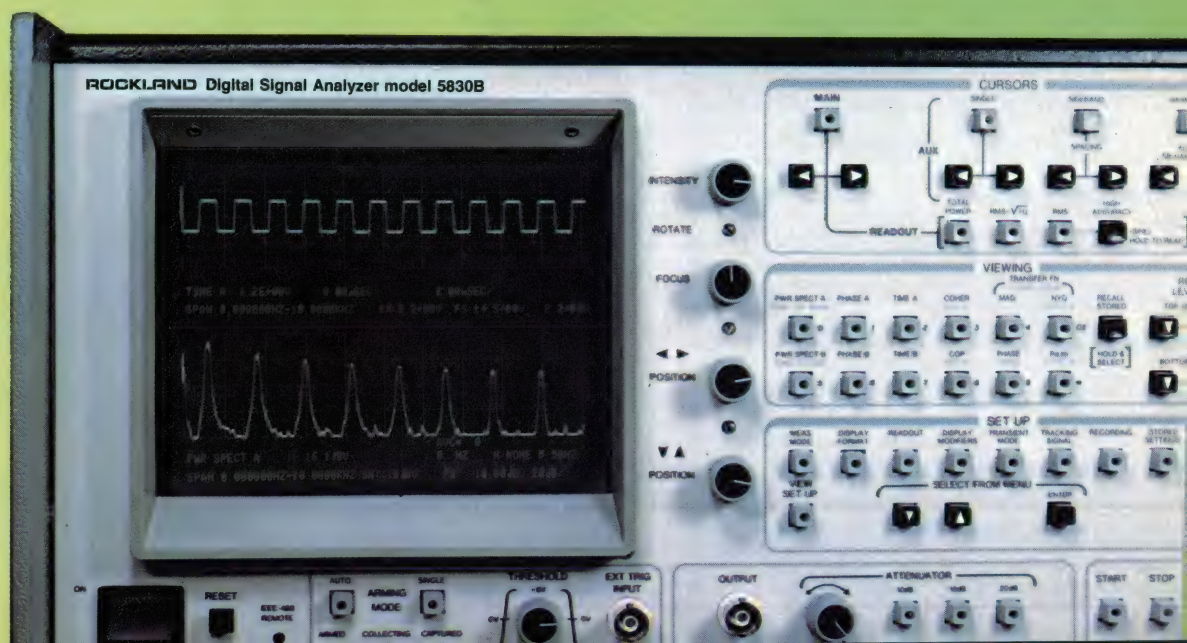
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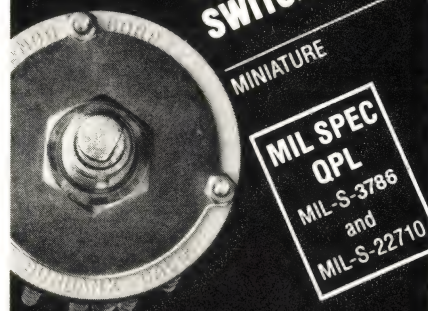
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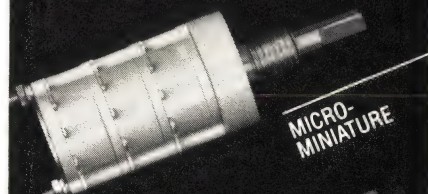


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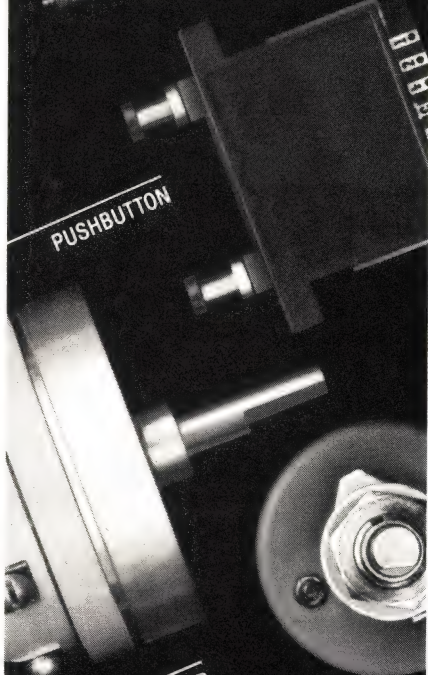


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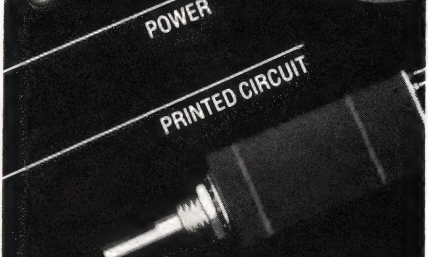
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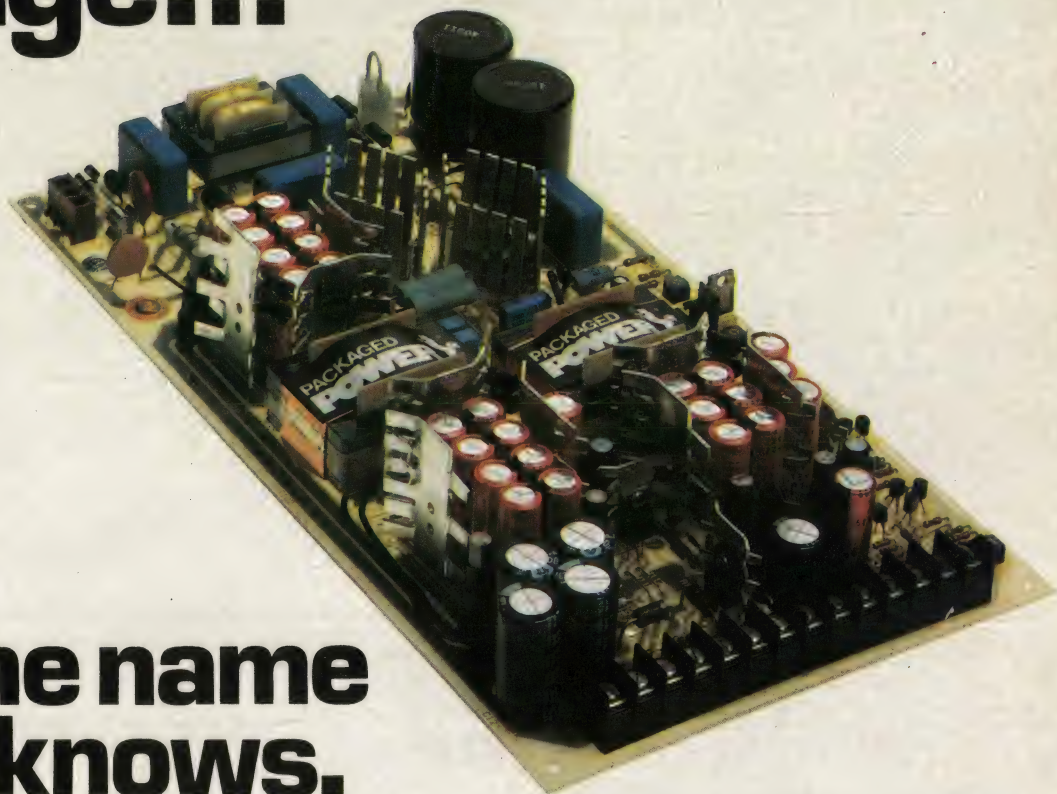
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Feb. 20	Jan. 24	Memory Technology; CAE; ATE (CAE-related*); Automated Design & Engineering for Electronics Product Preview (CAE-related*); Hardware & Interconnection Technology	
Mar. 6	Feb. 7	Semicustom IC (Array) Directory (CAE-related*); Communications ICs; Computer Board Directory; Connectors	Closing: 3/13
Mar. 20	Feb. 21	Test & Measurement; Analog ICs; Computer Peripherals; Support Chip Directory	
Apr. 3	Mar. 7	Communications Special Issue; Communications ICs; CAE; Buses; April Fools Supplement	Closing: 4/10
Apr. 17	Mar. 21	Power Supplies; Development Software; Memory Technology; Computer Graphics Devices (CAE-related*); Electro '86 Product Preview	

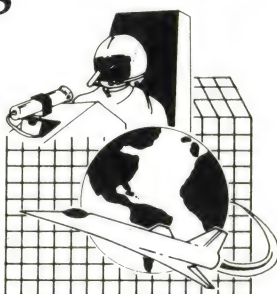
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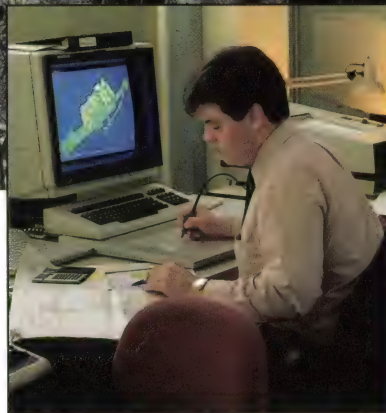
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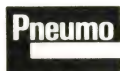
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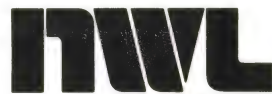
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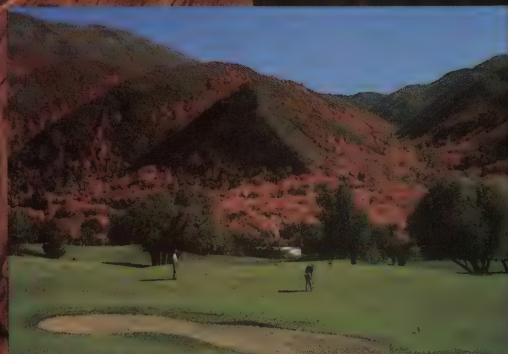
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The Science of Radar Image Processing

ERIM researchers are investigating numerous topics in the field of radar image processing, including speckle reduction and synthetic image generation.

Speckle Reduction

Due to the coherent nature of the synthetic aperture radar imaging process, radar images suffer from a disturbing speckle noise. This "salt-and-pepper" appearance of the imagery is a hindrance to the performance of radar image interpreters as well as automatic recognition algorithms. Conventional speckle reduction techniques, such as noncoherent integration of multiple looks and median filtering, degrade image resolution and thereby blur key image features such as edges and point returns.

To overcome this difficulty, ERIM researchers developed a nonlinear speckle reduction algorithm based on geometric concepts. The method iteratively applies a sequence of neighborhood processing operations based on the "digital convex hull". As shown below,

this algorithm preserves edges and strong returns in the image without resolution degradation while smoothing speckle.

Synthetic Image Generation

The ability to synthetically generate radar images of modelled objects has many important advantages. These include imaging of objects which do not physically exist, interactive object design via changing of object material properties or shape, and avoidance of costly sensor collections.

ERIM's staff have developed a hardware/software system capable of producing realistic radar images of modelled objects. A combinatorial solid geometry model of the object is first generated from available plans and photos. This model is then input to a module which emulates the electromagnetic interaction between radar and object. Important features such as multiple reflections, shadows, range layover and

added noise are faithfully portrayed in the resulting imagery. Extension of this capability to include IR and optical wavelengths is now underway.

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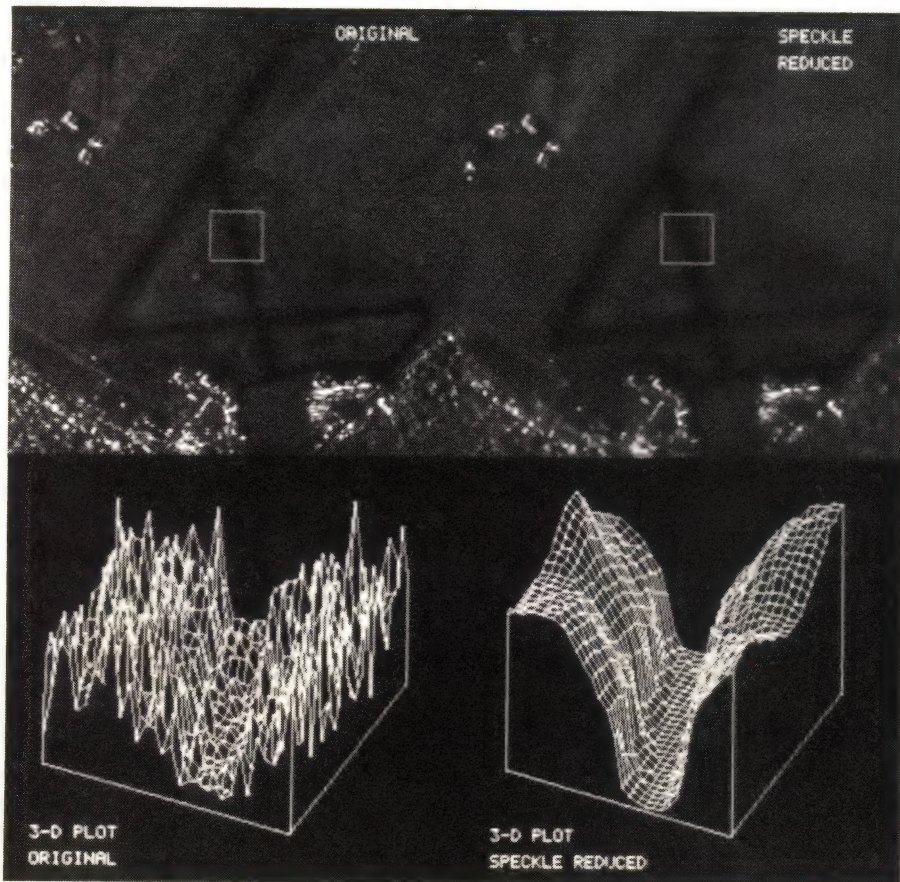
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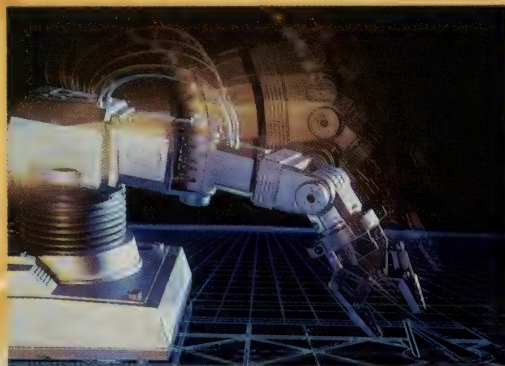
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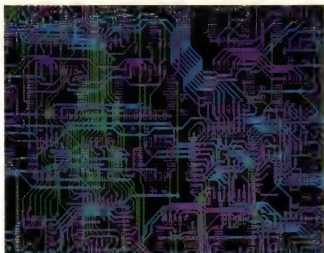
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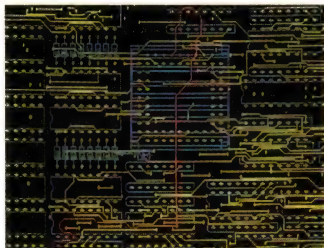
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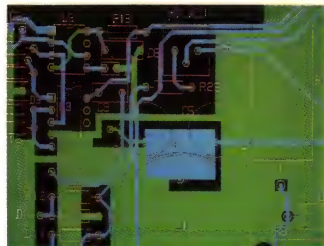
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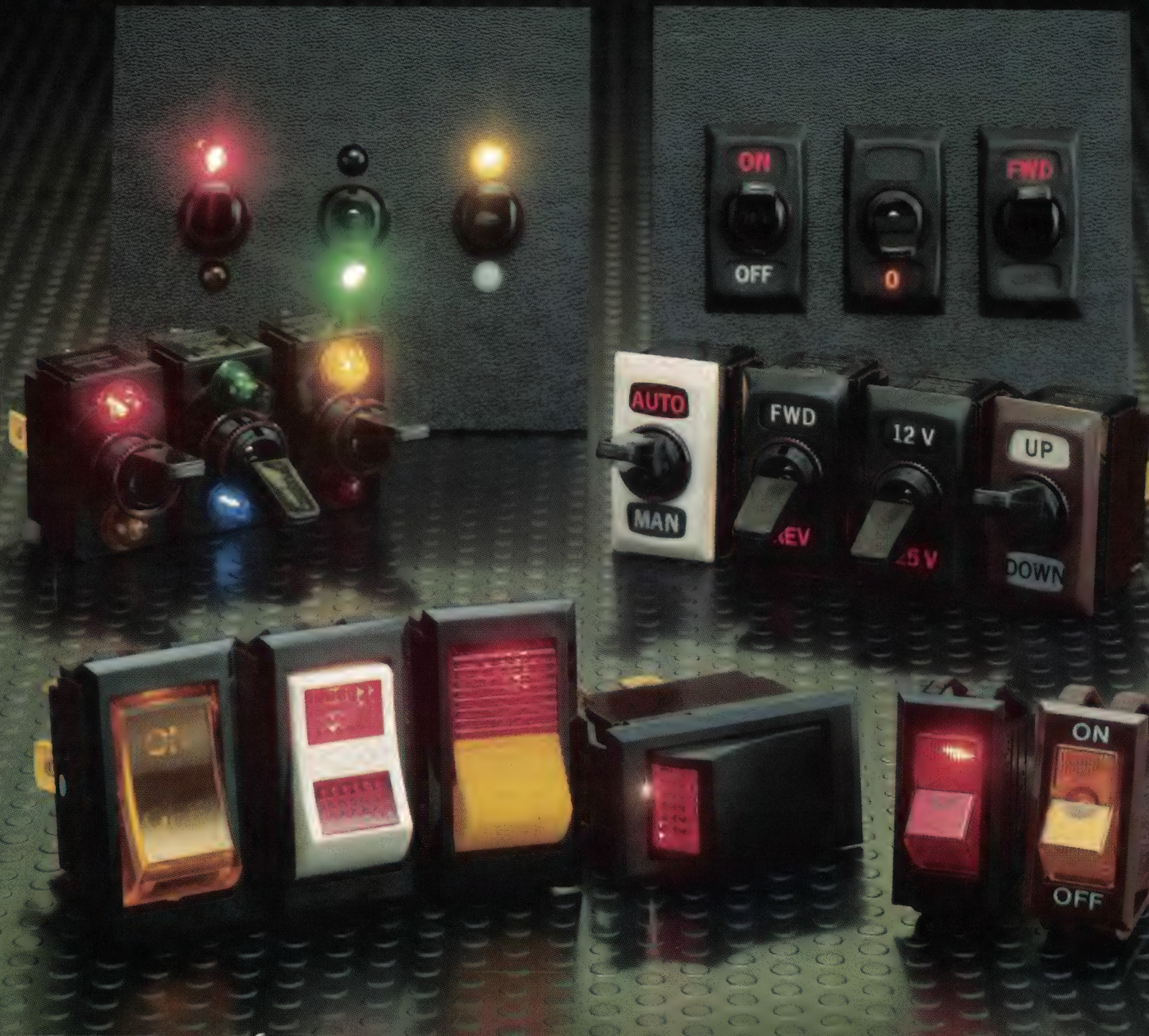
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LOOKING AHEAD

EDITED BY GEORGE STUBBS

'86 forecasts vary widely for semiconductor industry

Semiconductor industry watchers have issued a range of forecasts, from the bleak to the bountiful, concerning the industry's expected 1986 fortunes. Most projections, made last fall, suggest a move toward recovery, but they tend to fall short of predicting a return to typical industry growth rates. The most hopeful projection is for a 25% growth in total sales of semiconductors; the most pessimistic forecast sees a 2.5% drop in sales.

The 25% growth projection comes from the Semiconductor Industry Association (San Jose, CA). "We are continuing to see early signs that a semiconductor recovery has begun," said SIA president Thomas D Hinkelman last fall. "The book-to-bill ratio for analog integrated circuits, for example, is up for the seventh consecutive month, rising from 0.72 in January to 0.99 in July. The increases are not yet sufficient, however, to balance the declines in other product lines."

Hinkelman expressed faith that a 5 to 10% growth rate in electronic equipment sales in 1986 would substantially influence the market for semiconductors. "If these forecasts hold firm, there will be a strong semiconductor market recovery next year, which will yield at least a 25% increase in sales during 1986."

DM Data, a market-research firm based in Scottsdale, AZ, sees a 10 to 15% growth rate in semiconductor sales for 1986. According to president Howard Dicken, that rate of growth nears, but does not reach, the industry's customary annual growth rate of approximately 18% over the last 20 years.

Dicken acknowledges that there are still large inventories of semiconductors, and that prices will remain soft for a while, but there are signs of hope. "I'm hearing reports that people are seeing just a trickle of new orders coming back in. The

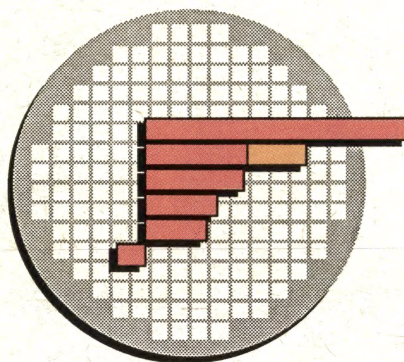
bookings have started to pick up." Dicken believes the current recession in the semiconductor industry has bottomed out, but even after the upturn, US makers will face problems in the form of a worldwide increase in capacity, thanks to the aggressive strategies of Japanese and Korean suppliers. In Dicken's eyes, it all adds up to some growth in the US, but less than the usual rate.

Integrated Circuit Engineering Corp (ICE), a Scottsdale, AZ, market-research company, is predicting 6% growth for the industry in 1986. ICE sees a 7% increase in unit volume and bases its forecast on a projection of stable average selling prices and "a relatively unexciting overall US economic picture"—ie, no recession but no boom. Forecasters at Dataquest Inc (San Jose, CA) echoed this view of the US economy.

According to Bill McLean, manager of market research at ICE, electronic equipment sales will increase by 6% in 1986, and he believes that a 6% or even an 8% growth rate in that sector would not yield a high rate of growth in the semiconductor industry unless prices went up. "I think there's just too much [manufacturing] capacity for that in '86," he remarked.

Of the forecasts given (see **Table**

TABLE 1— 1986 US SEMICONDUCTOR MARKET FORECASTS



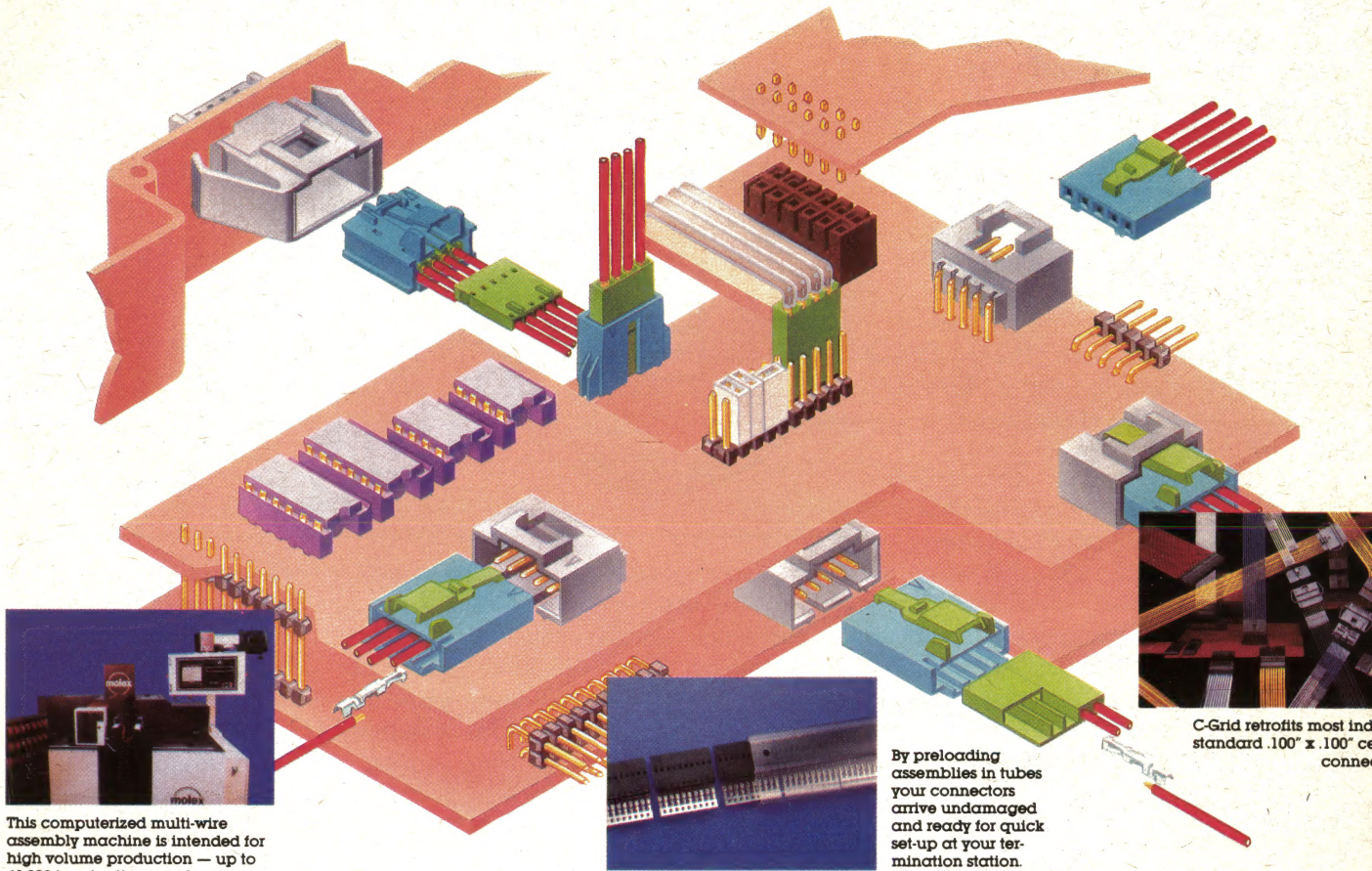
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1), In-Stat Inc's was the only one to project a negative growth rate. The Scottsdale, AZ, research company based its prediction of a -2.5% growth in part on its expectation of a sluggish US economy in 1986. According to vice president Jim Feldhan, the US Gross National Product will be up a humble 2.1%, and US businesses' pretax profits will be down from 1985's \$210 billion to \$190 billion.

Prices will remain soft in 1986, said Feldhan, and inventories will remain large, though more in the form of finished goods than raw stock. Lead times will be short: There's no incentive for buyers to make long-term commitments when devices are readily available and when prices will be stable or even decrease further.

Feldhen cited another reason to believe the industry won't be coming back strong in 1986. The semiconductor industry has weathered general recessions in the past by virtue of the popularity of certain types of consumer products, such as calculators, digital watches, and video games. Most recently, the boom in personal computers helped energize the industry. Although there are some good growth markets, no such captivating new product is on the horizon for 1986, said Feldhan.

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The modular interconnection system for maximum design flexibility at the lowest cost!

Today, circuit board packaging is becoming more complex. Your customers are growing more cost and quality conscious. To handle these increasing design demands, connector architecture too, must change.

Single/Dual Row Systems

This is why MOLEX has chosen to enhance its traditional .100" x .100" center post and receptacle product line. Now, in addition to breakaway headers, shunts and printed circuit board connectors, C-GRID boasts fully stackable, single piece IDT™ connectors, sixteen shrouded headers, and several panel mounts. To fulfill broader interconnect requirements, C-GRID has also been expanded into a completely modular product system — a feature

found nowhere else. Now discrete wire or cable assemblies can be stacked at a common rendezvous point and components can be independently disconnected as necessary. The result? Multi-piece interconnections are achieved as easily as two piece wire-to-wire or wire-to-board connections.

Automation Savings

Besides addressing the challenge of denser packaging, C-GRID can also be used in semi- or highly automated assembly equipment. The typical cost of a connector system is 30% connector and 70% labor. Significant manufacturing cost savings can be attained with our unique connector packaging and automated equipment. Furthermore, with automated assembly, the cost of field rejects are reduced to near zero since on-line testing verifies the integrity of each termination.

For existing and emerging electronic packaging problems, C-GRID is THE .100" x .100" system that integrates unique product design with automation capabilities.

Let us show you our system! Call the C-Grid desk, 312/969-4500 and ask for our 96-page C-Grid Catalog.

First in Customer Service ... Worldwide

molex

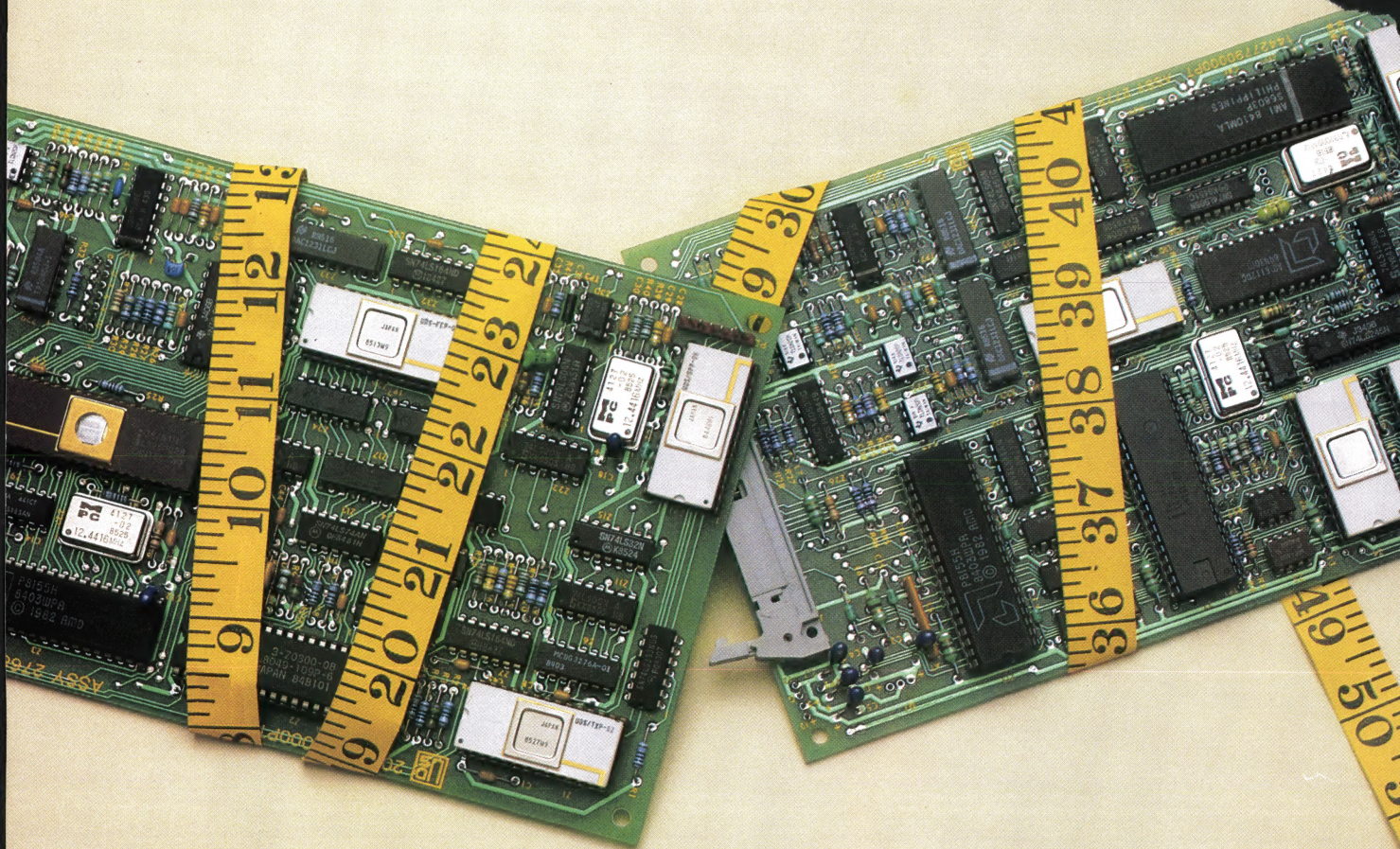
Corporate Headquarters: 2222 Wellington Court, Lisle, IL 60532 U.S.A. Phone: (312) 969-4550 Telex: 25-4069

European Headquarters: Molex House, Church Lane East, Aldershot Hants, GU11 3ST England Phone: (252) 318221 Telex: 851-858988

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CIRCLE NO 236

THE MODEM REDUCING PLAN THAT WORKED!



14.4kbps trellis coded and 9.6kbps modems on 40 square inches

LSI technology and UDS engineering expertise have combined to deliver two major improvements in modem design. Two of the most complex modems in the UDS product line—the fast-polling 9600FP and the Trellis Coded 14.4—have now been reduced to 40 square inches of board space for each complete modem. To accommodate varying OEM configurations, a wide variety of form-factor layouts and option packages is available.

9600FP

This UDS modem delivers 9.6kbps speed, with only 8ms turn-around time, making it ideal for fast-poll applications. A simple strap change puts the device into V.29 configuration, which includes alternative data rates of 7200 and 4800bps.

14.4 Trellis Coded

14.4kbps speed, merged with the signal-to-noise ratio enhancement of trellis coding, makes this modem your most cost-effective choice for moving large volumes of data over dedicated lines. It is particularly useful in applications such as complex

computer graphics, where error minimization is especially critical. The device has a fallback rate of 12kbps and is strappable to V.29.

These new OEM modem cards are small wonders! For technical details and quantity prices, contact Universal Data Systems, 5000 Bradford Drive, Huntsville, AL 35805. Telephone 205/837-8100; Telex 752602 UDS HTV.

 Universal Data Systems



MOTOROLA INC.
Information Systems Group

UDS modems are offered nationally by leading distributors. Call the nearest UDS office for distributor listings in your area.

DISTRICT OFFICES: Atlanta, GA, 404/998-2715 • Aurora, CO, 303/368-9000 • Blue Bell, PA, 215/643-2336 • Boston, MA, 617/875-8868 • Columbus, OH, 614/895-3025 • East Brunswick, NJ, 201/238-1515 • Glenview, IL, 312/998-8180 • Houston, TX, 713/988-5506 • Huntsville, AL, 205/837-8100 • Issaquah, WA, 206/392-9600 • Mesa, AZ, 602/820-6611 • Milwaukee, WI, 414/273-8743 • Minnetonka, MN, 612/938-9230 • Mountain View, CA, 415/969-3323 • Richardson, TX, 214/680-0002 • St. Louis, MO, 314/434-4919 • Silver Spring, MD, 301/942-8558 • Tampa, FL, 813/684-0615 • Thousand Oaks, CA, 805/496-3777 • Tustin, CA, 714/669-8001 • Uniondale, NY, 516/222-0918 • Willowdale, Ont, Can, 416/495-0008 • Ypsilanti, MI, 313/483-2682

CIRCLE NO 238

HOW TO RACE FASTER & LONGER DOWN THE DATA HIGHWAY

Approach The Speed of Light
with New
Extended Distance
Data Cables from Belden.

Set new standards in data transmission

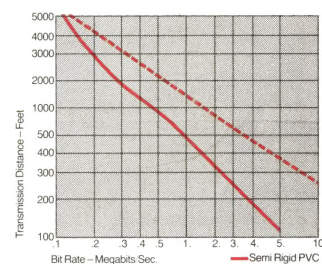
When data speed and distance set the limits to superior performance of your computer system, your design requires a new cable solution. Belden's new Extended Distance Data Cables provide faster data rates over longer distances while maintaining the integrity of the signal. This new series of data cables combines Belden's unique Datalene[®] foam dielectric or semi-rigid PVC insulation with superior shielding technology to achieve higher levels of performance than you

may have thought possible.

Choose from a wide selection of data cables in multipair or multi-conductor configurations. For capacitance levels as low as 12.5 pF/ft., specify Datalene insulation, available in conductor sizes of 24 and 28 AWG. Or request semi-rigid PVC insulation, offered in conductor sizes of 22, 24 or 28 AWG. All cables are shielded with foil and 65% braid for superior shielding effectiveness at both low and high frequencies. 24 AWG multipair cables are also available with individual pairs shielded in foil, plus an overall foil/braid shield for critical high noise applications.

Let Belden assist you with the selection of data cables to suit your system needs at the onset

Bit rate vs. distance for individually shielded single pair cables.



Charts assume 5% peak to peak time jitter as determined by eye pattern measurements of pseudorandom NRZ code.

of your design. This may help you avoid the need for costly overdesigned cable later on.

Settling a bit of confusion.

In general, low capacitance contributes to a better computer cable. However, at higher bit rates, the distance trade-off becomes more dependent on other cable parameters such as shielding, impedance and attenuation. "Low capacitance" can no longer define the performance requirements you need. Belden offers an examination of performance by addressing all parameters of data cables as they are affected across the bit rate spectrum in RS-232 and RS-422 applications. When it comes to optimizing performance, there is no equal to Belden.

Write or call Belden today for more information on our new Extended Distance Data Cables. Belden Electronic Wire and Cable, P.O. Box 1980, Richmond, IN 47375.

1-800-BELDEN-4

There is no equal.

Belden

CIRCLE NO 237



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